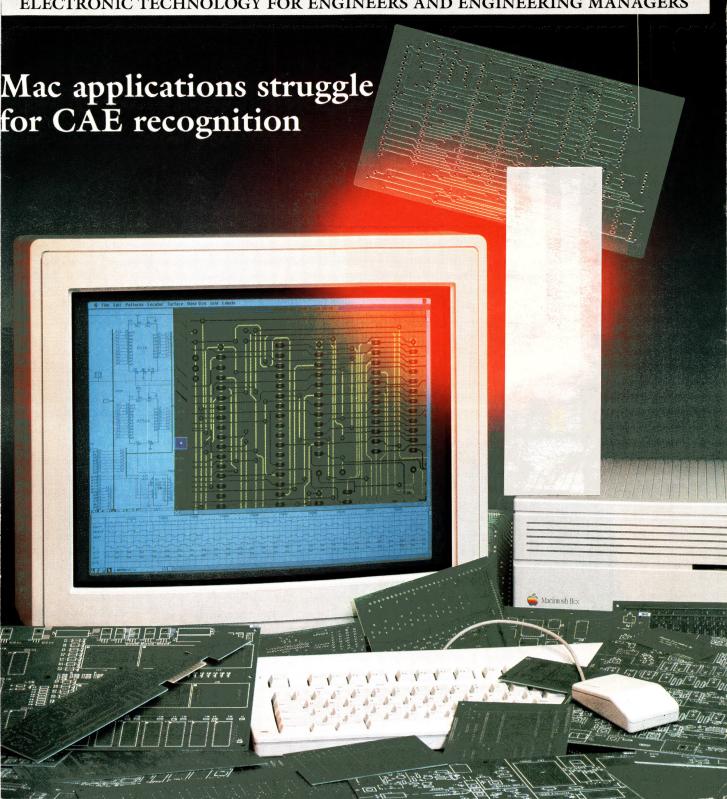
185 MAR 1980 esigner's guide to op-amp macromodels

> Nonstructured design for building testable ASICs

> > 4-bit microcontrollers suit diverse needs

> > > ROM emulation

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	27C210	64K×16	44	PLCC
2-Mbit	27C020	256K×8	32	CERDIP
2-MDIt	27C220	128K×16	40	CERDIP
4-Mbit	27C240	256K×16	40	CERAMIC

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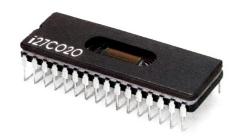
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As you can see from the chart, we're the EPROM source you've been looking for. Only Intel gives you the widest range of densities, from 16K to 4-Mbit. And that's just the beginning. We also let you choose byte-wide or word-wide architectures. PLCC or CERDIP packaging. And a range of speeds, from 120 ns to 200 ns.

But whichever Intel EPROM you choose, the benefits are obvious. Using one 2-Mbit instead of eight 256K EPROMs, for example, results in reduced board space, increased system reliability and

Now that we've been properly introduced.

Intel To Show 2-Mb, 4-Mb EPROMs

TOKYO - Intel Corp. chairman Gordon Moore will intro-duce his company's highest-density EPROMs at a press conference here tomorrow

Intel executives are flying to Tokyo to take the wraps off two 2-megabit EPROMs and one 4-Mbit EPROM to demonstrate company's commitment to the Japanese market.

Though Intel is the world's leading producer of EPROMs, the company owns less than 5% of Japan's EPROM market, said Tom Price, marketing manager of Intel's Programmable Mem-

ory Operation.

Intel owned 18% of the world's \$1.8 billion EPROM market in 1988, according to Dataquest Inc.

The Japanese market has been quick to pick up high-density EPROMs, Price said. and Intel is hoping to some market of

its 128 which is imes 8 (2-Mbit) part; and a 4-Mbit EPROM organized as 256-K imes 16, which will be in production in August.

Moore said these chips could reduce the number of memory chips in a system up to 75% while facilitating the design of

more-compact systems.
Fujitsu Ltd., NEC Corp. and Toshiba Corp. are the only manufacturers shipping either 2- or 4-Mbit EPROMs, according to Dataquest industry analyst Mary Olsson.
Though Japanese suppliers

made their public announce-ments of 2- and 4-Mbit EPROMs before Intel did, Price said Intel is determined to ramp very quickly to volume production.

Intel's swift ramp-up of its 2-and 4-Mbit EPROMs will bring selling prices down quickly terms of cost per ber



intel's Moore: In Japan to show his company's densest EPROMs.

K × 8 configuration costs apiece in 10,000-piece qu ties. Faster, 150-ns vers: all the new EPROMs wi for about 25% more.

The byte-wide (25¢ part comes in a 32-7 while the 16-bit-come in 40-pin co 32-pin and 40-pir the same ones Mbit EPRON word widths future EPP density

The Intel parts are all produced with the same 1-micron CHMOS process Intel uses to build 80386 microprocess

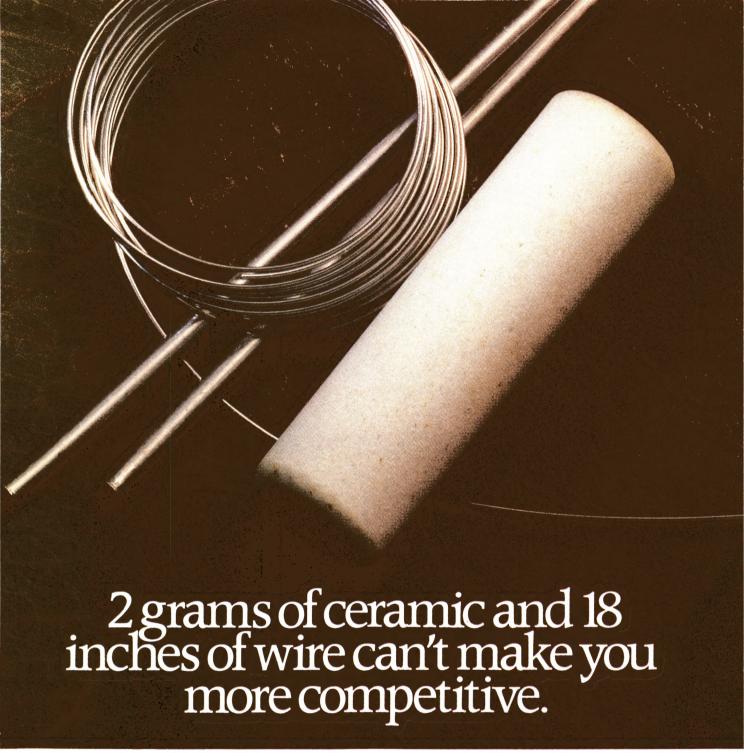
th the process line solds in the process line solds microproces any plans to the process of the sold in the process of the proces コンのようなシステムに適した アトをストアするパン さて、今回発養された Intel erweitert EPROM-Spektrum nach oben メモリだ。 ROMEN PORRESTA 2- una 4-mair-EPROMs in 1,0-µm-CMOS-Technologie もう1種類の2M EPROM EPKUMS IN 1,0 List PROM und zwei Architektur-Va2007
Ein 4-Megabit-EPROM und zwei Architektur-Va2007
Fin 4-Megabit-EPROM und zwei Architektur-V (256K×8)27C020は、高性能組 な込み制御ニステムなどに最適。 2- und 4-Mbit-EPROMS III */ PROM und zwei Intel vorgestelli.

© 1002 Ein 4-Megabit-EPROM und zwei Intel vorgestelli.

© 2-Megabit-Typs hat Intel vorgestelli.

© 2-Megabit-Eprom und zwei Intel vorgestelli.

© 2-Megabit-Typs hat Intel ト構成の27C240 たとえばベージブリンタのよう Die neuen Speicherbauelemente werden in 1-µm-CHMOSpie neuen zu den zu に、機能なアログラムや大量の コード配理に多数のEPROM schen 150 und 200 ns. Die bereits in Mustern verfügbaren schen 150 und 200 ns. Die bereits in Mustern verfügbaren Bausteine, deren Massenproduktion im August anläuft, sind auch im PLCC-Gehäuse erhältlich. を使用するシステムでの利用が 考えられる。(リザれもサンフル 出荷は始まっているが、星座に lichkeit vom 1-Mbit-Typ 27C210 えるのは今年9月から。 lichkeit vom 1. Mbit-Typ 27/210 1416 E Architektur ermöglicht E Architektur ermöglicht E Architektur ermöglicht E Architektur ermöglicht E インテルでは今後、メモリと FRELTEPROMES aen virtschaftlichsten und kom-paktesten Platinenentwurf für Das EPROM 27C240 ist ein paktesten platinenentwurt tur paktesten platinenen platin ンシュメモリを中心にゼジュ vas crkuri 2/240 isi Billi nichtlüchtiger Speicher mit ei-Systeme wie etwa resonar to computer, die lediglich ein ode to computer, die lediglich ein ode to to computer ein ode ein ode to computer ein ode to computer ein ode to computer ein ode to computer ein ode ein o を展開していくという。数 ner Kapazität von 4 Mbit, organer Kapazität von 4 Mbit, orga-nisiert zu 256K x 16 bit, und mit 150 oder 200 ns Zugriffszeit von 150 oder 200 ns Zugriffszeit ke-fügnik. Dit Gehäuse nach Jedec-granik. Dit Gehäuse nach Jedeccomputer, are redigitor ein oder zwei EPROMs zum Speicher. までDRAM に注し von Boot-Code oder BIOS Software benötigen. EPROM 27C210 im 40poligen
DIP. Um den unterschiedlichen Standard und ist aufwärtskom Standard und ist autwarrskom-patibel zu Intels 1-Megabit-EPROM 27C210 im 40poligen Das 2-Mbit-Erkoviv 8 bit und organisiert zu 256 K × 32poliger unteraebracht im DIP, eignet sich optimal für UIT. Um den unterschiedlichen Systemauslegungen und Pro-zessorbuserfordernissen entge-genzukammen, bietet Intel auf der 2-Mannhit Fhana mini Ander 2-Mannhit Fhana mini Ander Prostungsstorke Mikroprozessor Schaltungen mit zahlreichen, ir Speicherbänken angeordneter genzukommen, bierer intei aufder 2-Megabit-Ebene zwei Arthete an. Das EPROM chitekturen an. Das K bit of 17 C 220 ist zu 128 K x K bit of and kindet mit aufder and kindet mit aufder aufder aufder aufder aufder aufder auf Speicherbänken angewere Pro-EPROMs, die komplexe Daten-gramme oder grosse Typische speichern, Typische 2/CZZU ist zu 126 K. x 16 bit organisiert und bietet mit seinen 40poligen Keramik-DIP eben falls eine direkte Nachrüstmög mengen speichern.



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- VRTX32 multitasking executive designed for real-time embedded computer applications.
- GEN-960 for refining ROM or RAM code when setting up standalone embedded applications.
- ASM-960 assembler allows macroassembler users to fine tune application code as well as provide utilities for developing, debugging and maintaining application code.
- Intel and GNU compilers optimized for the 80960 family of embedded processors.

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SPECIFICATIONS				
Freq. Range(MHz)	TOSW-2 ZSDR-23 10-3000		TOSW-4 ZSDR-42 10-2500	
Insert. Loss (dB)	typ.	max.	typ.	max.
10-100MHz	1.3	1.9	1.3	1.7
100-1500MHz	1.1	1.9	1.1	1.7
1500-3000MHz	1.8	2.7	1.8	2.5
Isolation(dB)	typ.	min.	typ.	min.
10-100MHz	60	40	60	40
100-1500MHz	40	28	40	30
1500-3000MHz	35	22	35	22
1dB Compression(dBm)	typ.	min.	typ.	min.
10-100MHz	17	6	17	6
100-1500MHz	27	19	27	19
1500-3000MHz	30	28	30	28
VSWR(ON)	typ.	max.	typ.	max.
	1.3	1.6	1.3	1.6
Switching Time (µsec) (from 50% TTL to 90% RF)	typ.	max.	typ.	max.
	2.0	4.0	2.0	4.0
Oper. Temp.(°C)	-55 to +1	00	-55 to +1	00
Stor. Temp.(°C)	-55 to +1	00	-55 to +1	00
Price (10-24) (1-9)	\$39.95 \$89.95		\$59.95 \$109.95	

10 to 3000MHz from \$3995

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TO-8 package or a small EMI-shielded metal connectorized case, these tiny PIN-diode reflective switches, complete with driver, can operate over a 10 to 3000MHz span with a fast 2μ sec switching speed.

Despite their small size, these units offer isolation as high as 40dB(typ), insertion loss of only 1.1dB(typ), and a 1dB compression point of +27dBm over most of the frequency range. All models are TTL-compatible and operate from a dc supply voltage of 4.5 to 5.5 V with 1.8mA quiescent current.

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SURFACE MOUNT MIXERS



The opportunity for automated, low-cost assembly is a key benefit of surface-mount technology, but is often wiped out by

the high price of surface-mount components. Now, Mini-Circuits offers a new series of mixers to meet the pricing demands of SMT...only \$3.30 in 1,000 quantity (\$3.95 ea. in quantity of 10)...at a cost even lower than most conventionally-packaged mixers.

The SCM-1 spans 1 to 500MHz and the SCM-2 covers 10 to 1,000MHz. Housed in a rugged, non-hermetic 0.4 by 0.8 by 0.3 in. high (maximum dimensions) plastic/ceramic package. Spacing between connections is 0.2 in. The mixer is offered with leads (SCM-L) or without leads (SCM-NL) to meet a wide range of pc board mounting configurations.

Each SCM is built to meet severe environmental stresses including mechanical shock/vibration as well as temperature shock. The operating and temperature storage range is -55°C to +100°C. Each SCM, designed and built to meet today's demanding reliability requirements, carries Mini-Circuits' exclusive 0.1% AQL guarantee of no rejects on every order shipped (up to 1,000 pieces).

When you think SMT for low-cost production, think of Mini-Circuits' low-cost SCM mixers.

finding new ways ... setting higher standards

SPECIFICATION (typical)	ONS	SCM-1NL (L=with leads)	SCM-2NL (NL=no leads)
FREQ. RANGE (N LO,RF IF	ИHz)	1-500 DC-500	10-1000 5-500
CONVERSION LO Midband Total Range	OSS (d	B) 6.3 dB 7.5 dB	6.5 dB 8.0 dB
ISOLATION (dB) Low-Band Mid-Band High-Band		(L-R)(L-I) 60 45 45 40 40 35	(L-R)(L-I) 45 35 35 30 25 20
PRICE		(1000 qty) (1-9)	\$4.15 (1000 qty \$5.45 (1-9)

SCM-1L

SCM-2L

Units are shipped in anti-static plastic "tubes" or "sticks" for automatic insertion.

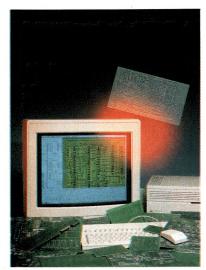
*NOTE: L & NL suffix for ordering only Not marked on units

Mini-Circuits

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March 1, 1990

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: An influx of new CAE/ CAD packages re-ignites debate over the Macintosh's capability as a workstation. Look for the Special Report on pg 138. (Photo courtesy Douglas Electronics Inc)

SPECIAL REPORT

Macintosh-based CAE

138

Macintosh zealots see the recent flurry of Mac-based CAE/CAD software releases as a torrent of new applications for their beloved system. Skeptics see these releases as too little too late to provide engineers with the depth of alternatives they need for real design work. Is the glass half full or half empty?—Michael C Markowitz, Associate Editor

DESIGN FEATURES

Designer's guide to Spice-compatible op-amp macromodels—Part 2

155

Part 1 of this article pointed out some deficiencies of the existing Boyle op-amp macromodel and described the structure of a new, modular macromodel for use with Spice-compatible circuit simulators. Part 2 describes the practical implementation, using the new structure, of models for two recent op amps; provides sample Spice net lists; and compares the simulation accuracy and computation time of the new models with those of the Boyle approach.—Mark Alexander and Derek F Bowers, Precision Monolithics Inc

Build testable ASICs using nonstructured design techniques

167

Due to the perceived penalties of designing for testability, designers often ignore the testability of their ASICs until late in the design phase. However, if you use nonstructured—as opposed to formal—design-for-test techniques, you can limit the risk of building untestable chips and improve the quality of your ASICs. —Daniel J Payne, Silicon Compiler Systems Corp

Continued on page 7

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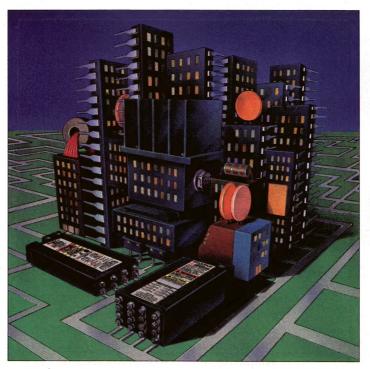
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Model	Output '	Voltage (V	DC) and M	aximum C	urrent
		(amp	eres) per C	hannel	
	#1	#2	#2	#6	#5

MOUCI	Output	Voltage (V	DC) and M	LAXIIII (urrent
		(ampe	res) per C	hannel	
	#1	#2	#3	#4	#5
Single Outpu	ut				
ST1-1401	2@120	Tota	Loutput po	wer may no	t evceed
ST1-1402	5@120			y model, sir	
ST1-1301	12 @ 50			out. Lower p	
ST1-1302	15 @ 40			els and man	
ST1-1303	24 @ 25			re available	
ST1-1304	28 @ 21		se contact t		
ST1-1305	48 @ 13				
Dual Output					
ST2-1401	2 @ 60	5@60			
ST2-1402	5 @ 60	5 @ 60			
ST2-1403	5 @ 60	12@33			
ST2-1404	12@33	12@33			
ST2-1405	15 @ 26	15 @ 26			
Triple Outpu	ut				
ST3-1401	5 @ 60	12 @ 16	12@16		
ST3-1402	5 @ 60	15@13	15@13		
ST3-1501	5@90	12 @ 8	12@8		
Quad Outpu	ıt ·				
ST4-1401	5@30	12 @ 16	12 @ 16	5 @ 30	
ST4-1402	5@30	15@13	15@13	5@30	
ST4-1403	5@30	12 @ 16	12 @ 16	24 @ 8	
ST4-1501	5 @ 30	15@13	15@13	24@8	
ST4-1502	5 @ 60	12 @ 16	12 @ 8	5@15	
ST4-1503	5 @ 60	15@13	15@7	5@15	
ST4-1504	5@60	12 @ 16	12 @ 8	24@4	
ST4-1505	5 @ 60	15@13	15@7	24@4	

STAKPAK STANDARD 1200 WATT MODELS



Model	Output	Voltage (V	DC) and M	laximum (urrent
		(ampe	res) per C	hannel	
	#1	#2	#3	#4	#5
Single Outp	ut				
SP1-1801	2 @ 240	Tota	Loutnut no	wer may no	t exceed
SP1-1802	5 @ 240			ny model, s	
SP1-1803	12 @ 100			out. Lower p	
SP1-1604	15 @ 80			and many	
SP1-1605	24 @ 50			re available	
SP1-1606	28 @ 42		se contact t		
SP1-1607	48 @ 25				
Dual Outpu	t				
SP2-1801	2@120	5 @ 120			
SP2-1802	5@120	5@120			
SP2-1803	5@120	12 @ 66			
SP2-1804	12 @ 66	12 @ 66			
SP2-1805	15 @ 53	15 @ 53			
Triple Outp	ut				
SP3-1801	5 @ 180	12@16	12 @ 16		
SP3-1802	5 @ 150	12@33	12 @ 16		
SP3-1803	5 @ 180	15@13	15@13		
SP3-1804	5 @ 150	15 @ 26	15@13		
Quad Outpu	ut .				
SP4-1801	5 @ 150	12 @ 16	12 @ 16	5@30	
SP4-1802	5 @ 150	15 @ 1°	15@13	5 @ 30	
SP4-1803	5 @ 150	12 @ 16	12 @ 16	24@8	
SP4-1804	5 @ 150	15@13	15@13	24@8	

SP5-1801

SP5-1802

15@13

24@8

12@16



Because of the advantages of ROM emulation, the technique is now showing up in such areas as PROM programming, µP-system in-circuit emulation, and logic analysis (pg 57).

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TECHNOLOGY UPDATES

ROM emulation reaches far-flung fields

57

There's far more to ROM emulation than the name suggests. You can still get plenty of simple, inexpensive ROM emulators, but the technique of ROM emulation is popping up in unexpected areas such as PROM programming, incremental compilers, μ P-system in-circuit emulation, and logic analysis.—Charles H Small, Senior Editor

4-bit microcontrollers: ICs combine µPs with myriad I/O options

69

Today's 4-bit microcontrollers offer almost unlimited combinations of core processors, memories, I/O functions, packaging, and operating characteristics. In addition to the wide variety of chips available, many devices also provide specialized functions such as phone dialers and television tuners.—Maury Wright, Regional Editor

Semicustom circuits: Analog-digital ICs provide versatility

91

Mixed-mode semicustom ICs combine analog and digital functions on one chip, freeing system designers from the inherent limitations of early semicustom arrays. Although early mixed-mode chips are still available and often useful, today's devices generally offer superior performance.—Dave Pryce, Associate Editor

Analog comparators mate with ECL, TTL

115

Neither TTL nor ECL is a clear-cut winner in the battle for supremacy in IC design. ECL still maintains its edge in speed, though lower-power TTL circuitry is making steady advances in this crucial parameter. Manufacturers of analog comparators are covering their bets by developing new products that satisfy both the TTL and ECL camps. —Bill Travis, Contributing Editor

Continued on page 9

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At last, a <u>real</u> breakthrough design

What would the perfect PLD design software include?

Some problems are better solved using truth tables. Others could use a procedural language for state machines. Boolean equations are certainly necessary. Simplifying and condensing equations, especially repetitive ones, would be

OrCAD/PLD can do all of that.

It would have to work within schematics so documentation would all be in one place.

OrCAD/PLD does that, too.

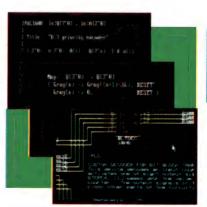
For output, you need to have a IEDEC file for PLDs and a hex file for PROM burning.

It's easy with OrCAD/PLD.

And logic synthesis? You don't want to buy extra hardware to handle something as complex as that.

OrCAD/PLD offers a whole new way of design expression called numerical mapping. Its the most powerful means for designing PLDs on any platform, yet it runs on a standard PC.

The perfect programmable logic design software shouldn't cost a lot.



Accepts multiple inputs, including truth tables, state machines, Boolean equations, indexed equations, schematic entry and numerical mapping

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EDN March 1, 1990

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Now there's a new plotter that makes output bottlenecks disappear. With the ColorStation D™ from Raster Graphics you can now generate wideformat color plots in minutes instead of hours. All for a starting price of \$18,500.

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Raster Graphics' ColorStation is engineering D-size (22x34), and comes standard with both RS-232 and Centronics interfaces. That

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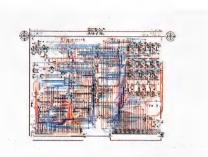
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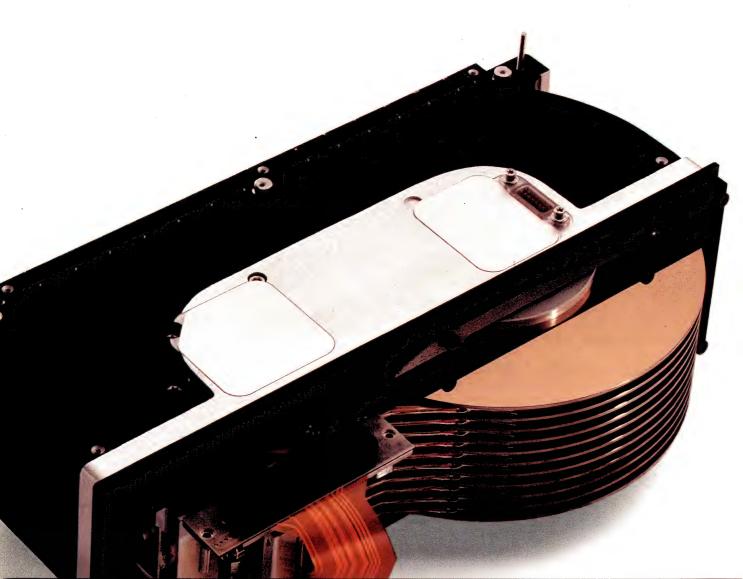
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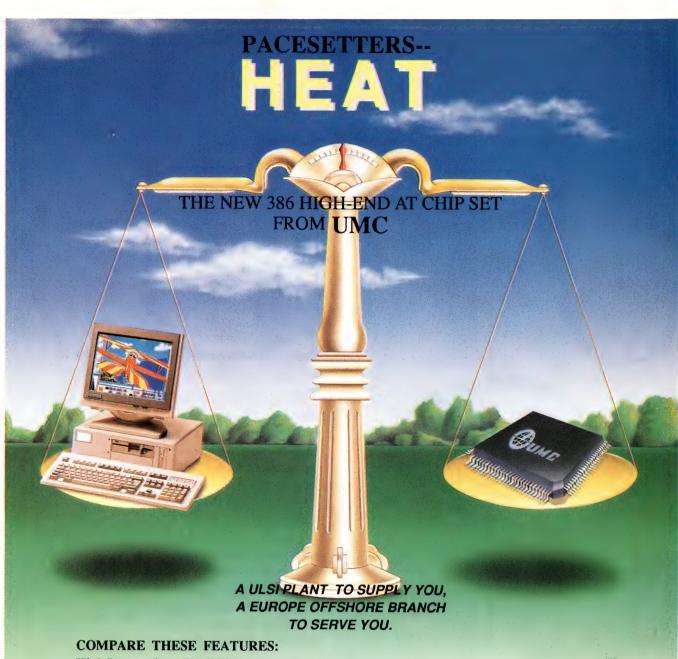
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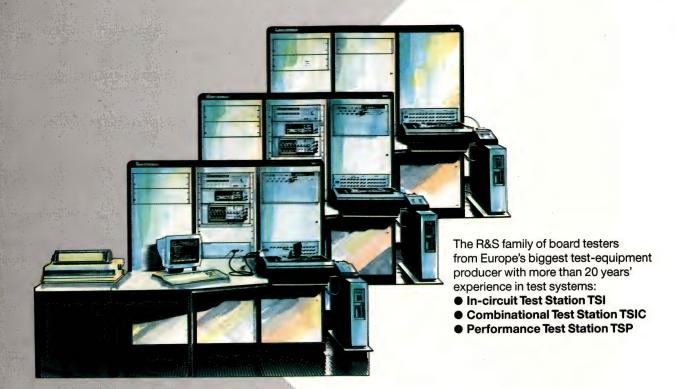
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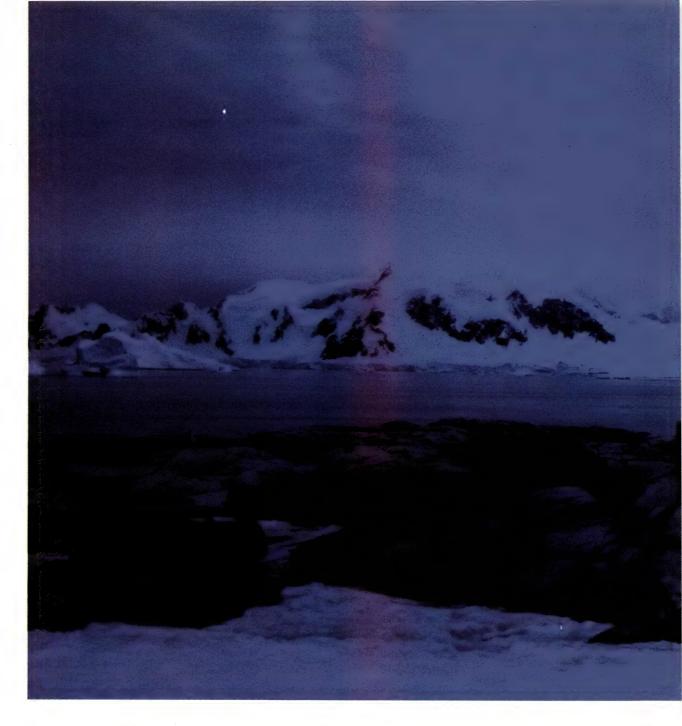
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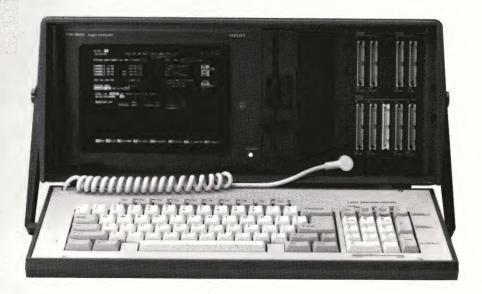
Fluke Breaks Tradition with Timely RISC Logic Analyzer Solution

Development of design and debug tools for microprocessors traditionally lags behind the introduction of the "new" chips the tools are designed to support. Thus, when the need for emulator or logic analyzer support is greatest, no help is available.

No longer is that true. John Fluke Manufacturing Company, Inc., has broken tradition by providing design engineers with timely support for the newest embedded controller on the market today. On the same day Intel launched its new i960 CA 32-bit RISC processor, Fluke introduced its PM 3655/R, a RISC Logic Analysis system that provides logic analyzer support and chip debug at full bus speeds for the i960 CA. Because Fluke was ready with this support system, Intel customers can immediately take full advantage of the i960 CA and its potential for advancing the state-of-the-art in many industries.

At 66 MIPS, the Intel processor demands high-performance from a logic analyzer. Fluke's PM 3655/R easily keeps pace. It features 100 MHz state performance and timing on 96 channels with 2 K-bits of memory per channel, set-up and hold times of less than 2.5 nanoseconds, complex triggering on four levels, and high impedance probes of 8 pf cap. and 1 M Ω resistance.

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PM 3655 Logic Analyzer

Also, its built-in MS/DOS operating system can post-process the logic analyzer data for disassembly or reformat it for use with ATE systems, workstations or applications programs.

The PM 3655/R package includes a new, powerful second-generation custom disassembler program. It provides mathematic capabilities, can handle nested translation tables and the use of internal variables. These features allow a user to generate a disassembler within a few days for virtually any processor.

The custom disassembler comes with a library of support for the Harris RTX 2000, Intel's 8031/51 and the IEEE-488 bus as well as for other microprocessors.

The PM 3655/R RISC Logic Analysis system is available for \$13,200; smaller configurations are available starting at less than \$6,000.

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CIRCLE NO. 29

NEWS BREAKS

EDITED BY JULIE ANNE SCHOFIELD

LOW-COST INSTRUMENT AMPS PROVIDE FOUR GAIN SETTINGS

Two digitally programmable instrumentation amplifiers from Burr-Brown Corp (Tucson, AZ, (800) 548-6132) each provide four gain settings. The PGA202 offers gain settings of 1, 10, 100, and 1000; the PGA203 provides gains of 1, 2, 4, and 8. The amps settle to 0.01% in 2 µsec, and their bandwidths are nearly constant with gain (1 MHz for gains less than 1000 and 250 kHz for a gain of 1000). Laser trimming sets both gain and offset characteristics, thus eliminating the need for external trimming components. The devices cost \$6.95 (100).—Steven H Leibson

MOUSE TAKES THE SHAPE OF A PEN

You can easily sign your name with the MousePen, a pen-shaped mouse from International Machine Control Systems (Paso Robles, CA, (805) 239-8976). You can use this 2-button serial mouse with IBM PC/XT, PC/AT, PS/2, and compatible computers. The mouse has a dynamic gain of 50 to 1000 pulses/in. built into the hardware. Slow movements give you low gain for precision positioning; fast movements give you high gain for rapidly moving the cursor across a screen. The MousePen, adapters for both DB9 and DB25 serial ports, and a Microsoft-compatible software driver cost \$129.—Doug Conner

CONTINUOUS-TIME FILTER IC HANDLES SIGNALS TO 4 MHz

A programmable filter IC introduced by International Microelectronic Products (San Jose, CA, (408) 432-9100) handles megahertz frequencies without aliasing. Rather than using switched-capacitor or other digital techniques, the IMP4520 continuous-time filter uses voltage-controlled resistors to set its frequency response. By using a serial programming port, you can set the 4-stage filter's poles from 100 kHz to 4 MHz and its zeros as great as 8 MHz. The filter will hold its response to $\pm 3\%$. You can reduce the filter's order by programming it to bypass any sections you don't need. The filter operates on 0 to 5V differential signals and draws 100 mA. It costs \$18 (1000); samples will be available in April.—Richard A Quinnell

DSO-BANDWIDTH WARS CONTINUE

In what has become almost a monthly event, the bandwidth of digital storage oscilloscopes has increased once again. For the moment, the fastest product is Hewlett-Packard's (Colorado Springs, CO, (800) 752-0900) \$42,800 54124T, which has a bandwidth of 50 GHz on two of its four channels. But, if history is any indication, Tektronix (Beaverton, OR, (800) 835-9433), whose 40-GHz CSA 800 series had previously held the crown, will soon counter with an even faster product. In announcing the 54124T, the company responded to Tektronix's 1989 introduction of differential time-domain reflectometry, a technique useful for characterizing balanced transmission lines. But unlike Tektronix, whose 11800 series uses matched, opposite-polarity pulse generators, Hewlett-Packard makes differential time-domain-reflectometry measurements using a single generator. As you might expect, each company claims advantages for its technique.—Dan Strassberg

EDN March 1, 1990

NEWS BREAKS

DEVELOPMENT SYSTEM FOR FPGAs SPEEDS DESIGN COMPLETION

If you're considering field-programmable gate arrays (FPGAs) for your next circuit, take a look at the development systems offered by Texas Instruments (Dallas, TX, (800) 232-3200). The Action Logic System (TI-ALS) software-based design-development tool lets you take an FPGA design from concept to silicon in a matter of hours. The tool includes a validator, which examines your design for adherence to design rules; a static timing analyzer; and user-definable stimulus vectors. It functionally tests and debugs your design and accepts net lists in a variety of input formats. Prices range from \$7950 to \$11,950, depending on the computer you use and whether you want an FPGA programmer.—J D Mosley

CPUs, PACKAGING, AND SOFTWARE HIGHLIGHT BUSCON

Motorola Microcomputer Div (Tempe, AZ, (602) 438-3000) announced at Buscon that it now offers the VMEbus MVME165 single-board computer based on the 32-bit (25- or 33.3-MHz) MC68040 μ P. The board hosts as much as 16M bytes of dynamic RAM and 256k \times 16 bits of EPROM. Other features include 8k bytes of nonvolatile RAM, a time-of-day clock, two RS-232C ports, and five timers. A master/slave VSB interface couples the board with other processors and high-speed memory. The VMEbus interface supports 32-bit address and data paths and includes the 7-level VMEbus Interrupter and Interrupt Handler and the 4-level VMEbus Requester. Expect to see the board in June at a base price of \$3995.

Low cost and modular design are the key features of the TSVME 110 single-board CPU, another product announced at Buscon, from Themis Computer (Pleasanton, CA, (415) 734-0870). The company offers the VMEbus-based board with an 8-MHz 68000 μ P, 64k bytes of static RAM, seven other EPROM/RAM sockets, two serial ports, a timer, and a real-time clock for prices as low as \$589 (100). You can also buy the board with a 10-MHz 68010 μ P. Options you can add via expansion modules include a floppy-disk controller, SCSI interface, as many as 2M bytes of dynamic RAM, and a rechargeable battery.

And Ampro Computers (Sunnyvale, CA, (408) 734-2800) has once again reduced the package footprint required to implement an industry-standard computer. The company now offers the IBM-compatible 80386-based Little Board/386 computer, which measures 5.75×8 in.—the same size as a 5^1 4-in. disk drive. The board includes a 20-MHz CPU, as many as 4M bytes of RAM, a floppy-disk controller, a clock, two serial ports, a parallel port, and a SCSI interface. It costs \$1170 (100) without RAM. You can add features to the board, such as the \$226 (100) VGA graphics controller, via the MiniModule expansion bus.

On the software front, Gespac (Mesa, AZ, (602) 962-5559) now offers its G-Windows package independently of its G-64 bus boards. The graphics package operates with Microware Systems' (Des Moines, IA, (515) 224-1929) OS-9 real-time operating system and provides developers with the tools to create graphics-based application software. The G-Windows-PP port pack costs \$2995; purchasers must also buy at least 10 end-user licenses at \$495 each. Gespac will offer a VMEbus graphics board to host the graphics software in June for approximately \$1900.—Maury Wright

AN ACME EDITORIAL

"Commitment is the key to any lasting partnership - when both sides share an enlightened self-interest, the relationship is bound to prosper."

The 1990's are upon us, ushering in a new age of cost-Conscious single-source suppliers and long-term supplier/ manufacturer relationships. Oddly enough, the philosophy behind this "new age" is anything but new. It has its roots in old-fashioned values. Values which stress the importance of commitment to a relationship. Values which acme Electric intends to build upon- today and in the years to come.

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NEWS BREAKS

IC-LAYOUT TOOL ROUTES THREE OR MORE LAYERS

Anticipating the growing use of three layers of metal interconnect on ICs, Cadence Design Systems (San Jose, CA, (408) 954-7533) introduced Cell3 Ensemble, a place-and-route layout system that supports both mixed-block and standard-cell designs. The software is compatible with CMOS, ECL, and BiCMOS technologies, and using it with a 3-level-metal process will increase circuit density, improve performance, and lower die cost. Timing-assurance and clock-tree-synthesis options augment the place-and-route software. Cell3 Ensemble is available now for most workstations; prices start at \$100,000.—Michael C Markowitz

ANNUAL VHDL USERS GROUP MEETING TO BE HELD IN BOSTON

The VHDL Users' Group (San Francisco, CA) will hold its third annual spring meeting in Boston, MA, on April 4 to 6. The meeting is open to anyone interested in VHDL, the VHSIC Hardware Description Language. It will feature half a day of tutorial seminars followed by two-and-a-half days of technical sessions focusing on the practical applications of VHDL. The meeting will also include a Thursday evening reception at Boston's Computer Museum. For more information about the meeting, contact Conference Management Services at (415) 329-0510.—Steven H Leibson

DATA-ACQUISITION BOARDS ELIMINATE USER ADJUSTMENTS

Data Translation Inc (Marlboro, MA, (508) 481-3700) introduced three data-acquisition boards that—compared with their predecessors—eliminate eight manual adjustments and more than a dozen configuration jumpers. Without operator intervention, the DT2831 Series boards calibrate themselves when you apply power and periodically thereafter. Despite this added complexity, the addition of a pair of counter/timers, and the fact that the company is shipping software drivers at no cost, pricing for the IBM PC/AT bus-compatible boards begins at \$995—the same as that of the previous product line. Each board has an amplifier with eight software-programmable gains, a 12-bit ADC that accommodates 16 single-ended or eight differential inputs, two 12-bit DACs, and eight digital I/O lines. The fastest member of the family, the DT2831-G, transfers data to memory under DMA control at 250k samples/sec. At its highest sensitivity, the DT2835 has a full-scale range of 20 mV.—Dan Strassberg

8051-BASED μC BOASTS 32k-BYTE EPROM

Popular μ C (microcontroller) architectures never die, they evolve as IC fabrication technology improves. The 87C51FC μ C from Intel Corp (Santa Clara, CA, (800) 548-4725) represents just such a device. At its core is an 8051 processor augmented with 32k bytes of EPROM, 256 bytes of RAM, a programmable counter array (PCA), three 16-bit timer/counters, and a 2-level memory-locking scheme for piracy protection. The PCA incorporates a separate 16-bit timer/counter coupled with an array of compare/capture modules, which provide precise timing control without direct CPU intervention. The memory-locking scheme comprises two program-memory lock bits and a 32-bit encryption table. The μ C maintains pin compatibility with older members of the 8051 family. The 12-MHz version costs \$67; the 16-MHz part costs \$73 (1000).—Steven H Leibson

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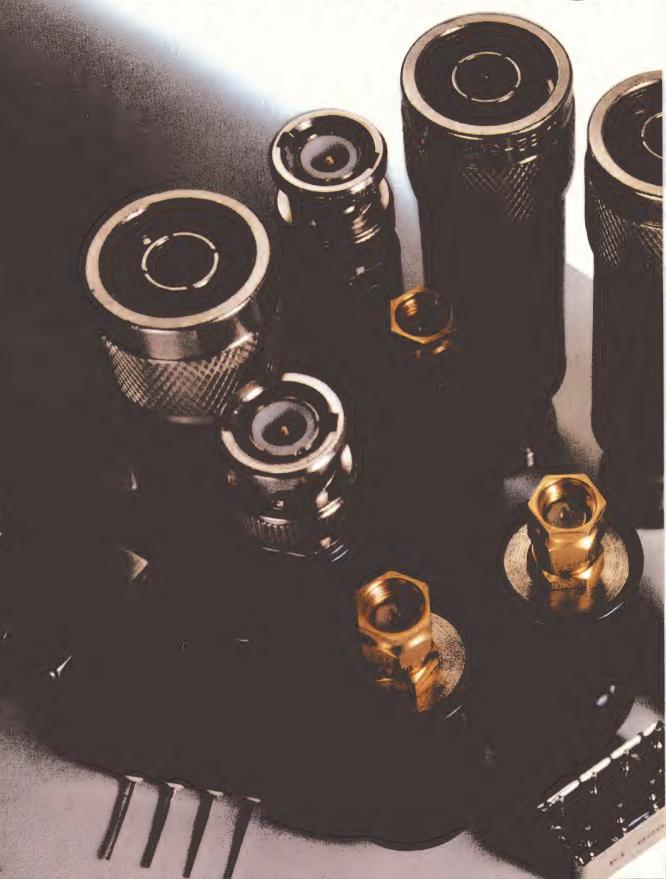
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EDN March 1, 1990



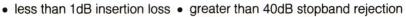
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FILTERS



dc to 3GHz from \$1145

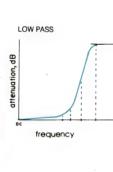
lowpass, highpass, bandpass, narrowband IF

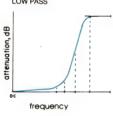


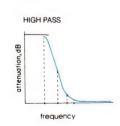
5-section, 30dB/octave rolloff • VSWR less than 1.7 (typ) • meets MIL-STD-202 tests

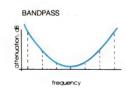
rugged hermetically-sealed pin models • BNC, Type N; SMA available

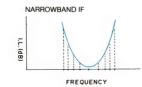
surface-mount • over 100 off-the-shelf models • immediate delivery











low pass dc to 1200MHz

	PASSBAND, MHz	fco, MHz	ST	VS	PRICE			
	(loss <1dB)	(loss 3db)	(loss>2	20dB) (loss	>40dB)	pass-	stop-	\$
MODEL NO.	Min.	Nom.	Max.	Max.	Min.	band	band	Qty. (1-9)
NO.	MIII.	NOITI.	Max.	Max.	WIII.	typ.	typ.	(1-3)
PLP-10.7	DC-11	14	19	24	200	1.7	18	11.45
PLP-21.4	DC-22	24.5	32	41	200	1.7	18	11.45
PLP-30	DC-32	35	47	61	200	1.7	18	11.45
PLP-50	DC-48	55	70	90	200	1.7	18	11.45
PLP-70	DC-60	67	90	117	300	1.7	18	11.45
PLP-100	DC-98	108	146	189	400	1.7	18	11.45
PLP-150	DC-140	155	210	300	600	1.7	18	11.45
PLP-200	DC-190	210	290	390	800	1.7	18	11.45
PLP-250	DC-225	250	320	400	1200	1.7	18	11.45
PLP-300	DC-270	297	410	550	1200	1.7	18	11.45
PLP-450	DC-400	440	580	750	1800	1.7	18	11.45
PLP-550	DC-520	570	750	920	2000	1.7	18	11.45
PLP-600	DC-580	640	840	1120	2000	1.7	18	11.45
PLP-750	DC-700	770	1000	1300	2000	1.7	18	11.45
PLP-800	DC-720	800	1080	1400	2000	1.7	18	11.45
PLP-850	DC-780	850	1100	1400	2000	1.7	18	11.45
PLP-1000	DC-900	990	1340	1750	2000	1.7	18	11.45
PLP-1200	DC-1000	1200	1620	2100	2500	1.7	18	11.45

high pass dc to 2500MHz

g p								
MODEL NO.		ND, MHz <1dB) Min.	fco, MHz (loss 3db) Nom.	STOP B (loss>20dB) Min.	AND, MHz (loss>40dB) Min.	pass- band typ.	wR stop- band typ.	PRICE \$ Qty. (1-9)
140.	IVIII I.	191111.	140111.	141111.				
PHP-50	41	200	37	26	20	1.5	17	14.95
PHP-100	90	400	82	55	40	1.5	17	14.95
PHP-150	133	600	120	95	70	1.8	17	14.95
PHP-175	160	800	140	105	70	1.5	17	14.95
PHP-200	185	800	164	116	90	1.6	17	14.95
PHP-250	225	1200	205	150	100	1.3	17	14.95
PHP-300	290	1200	245	190	145	1.7	17	14.95
PHP-400	395	1600	360	290	210	1.7	17	14.95
PHP-500	500	1600	454	365	280	1.9	17	14.95
PHP-600	600	1600	545	440	350	2.0	17	14.95
PHP-700	700	1800	640	520	400	1.6	17	14.95
PHP-800	780	2000	710	570	445	2.1	17	14.95
PHP-900	910	2100	820	660	520	1.8	17	14.95
PHP-1000	1000	2200	900	720	550	1.9	17	14.95

bandpass 20 to 70MHz

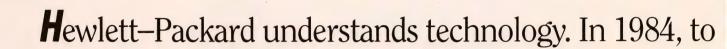
MODEL NO.	CENTER FREQ. MHz F0	PASS BA (loss < Max. F1	ND, MHz <1dB) Min. F2	(loss > Min. F3		AND, MHz (loss > 2 Min. F5		VSWR 1.3:1 typ. total band MHz	PRICE \$ Qty. (1-9)
PIF-21.4	21.4	18	25	4.9	85	1.3	150	DC-220	14.95
PIF-30	30	25	35	7	120	1.9	210	DC-330	14.95
PIF-40	42	35	49	10	168	2.6	300	DC-400	14.95
PIF-50	50	41	58	11.5	200	3.1	350	DC-440	14.95
PIF-60	60	50	70	14	240	3.8	400	DC-500	14.95
PIF-70	70	58	82	16	280	4.4	490	DC-550	14.95

narrowband IF

MODEL	CENTER FREQ. MHz	PASS BAND, MHz I.L. 1.5dB max.		ND, MHz 20dB		P BAND, MHz L. > 35dB	PASS- BAND VSWR	PRICE \$ Qty.
NO.	F0	F1-F2	F5	F6	F7	F8-F9	Max.	(1-9)
PBP-10.7 PBP-21.4 PBP-30 PBP-60 PBP-70	10.7 21.4 30.0 60.0 70.0	9.5-11.5 19.2-23.6 27.0-33.0 55.0-67.0 63.0-77.0	7.5 15.5 22 44 51	15 29 40 79 94	0.6 3.0 3.2 4.6	50-1000 80-1000 99-1000 190-1000 193-1000	1.7 1.7 1.7 1.7	18.95 18.95 18.95 18.95 18.95

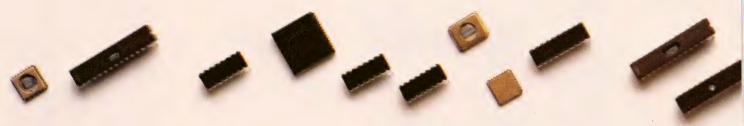
CIRCLE NO. 38



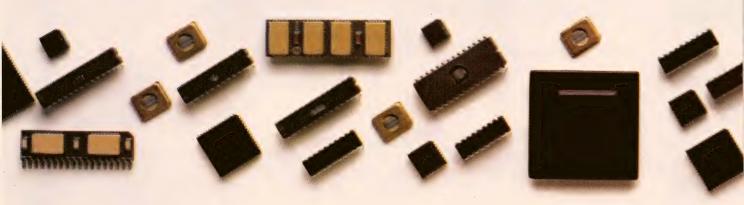




HP qualified a radical new CMOS part from a young



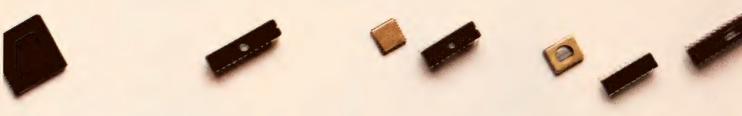
have matured. Today, we supply over 100 different



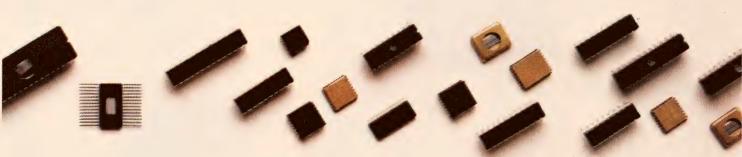
from mainframes to medical instruments..



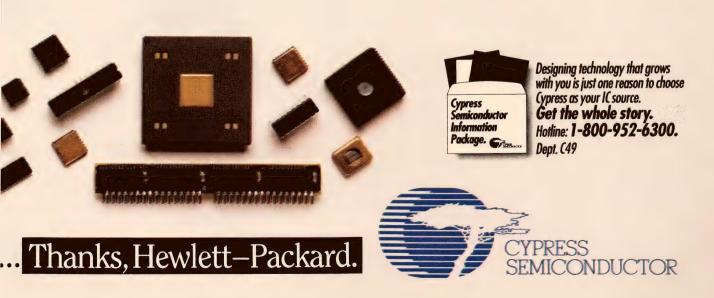
foster technology innovation for higher performance,



company. That technology and business relationship

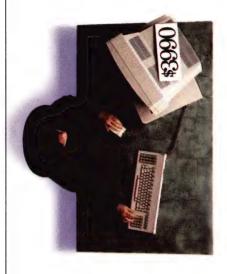


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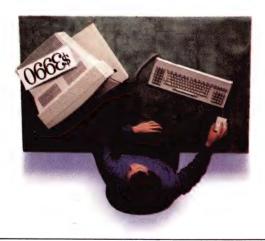






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EDN March 1, 1990 CIRCLE NO. 39 31



SIGNALS & NOISE

Following the lead to a new theory

I would like to comment on the letter from Steven L Comee (EDN, December 7, 1989, pg 33). It's not unusual for "counterestablishment" theories to be ridiculed. Max Planck's theory met with much skepticism initially, mainly because it was of an ad hoc nature; that is, it was tailored to fit specific facts. Scientists prefer a theory that predicts hitherto unknown facts that can be looked for through experimentation and, if found, lead to acceptance of the theory.

Steve's theory could be faulted if (a) his mathematical argument is erroneous, or (b) his theory does not lead to predictions that can be verified by suitable experiment.

Personally, I would like to see his theory. If the math hangs together, and if it can predict, then it is respectable and should receive serious consideration. It is stupid to laugh at theories just because you espouse some other cause. Nobody laughed louder than the flat earthers did.

Incidentally, Steve would probably have an ally in Edward Fredkin, who is a very successful computer expert, a self-made millionaire, and a one-time professor at the Massachusetts Institute of Technology. He thinks the universe is a computer. That did not stop him from becoming a millionaire, and Steve Comee should not be satisfied that there is no money in his own ideas.

Frank L Morris Arlington, TX

He knows the feeling

In response to Mike Markowitz's editorial, "Cut us in on profits, too" (EDN, November 23, 1989, pg 47), haven't we all felt that way at some time or another, especially when some semiliterate athlete receives 4 or 5 million just for signing with

a professional team?

Recently, a colleague told me about a schoolmate who had failed engineering but managed to receive a degree in business. It seems that this kid, five years out of college, made half a million dollars on Wall Street last year, trading futures.

Does this reflect, among engineers, a tragic lack of entrepreneurial ability that "goes with the territory?" Or is it a predisposition that eschews activity smacking of commercialism? (Really, Michael, could you see yourself making a career out of slam-dunking a hollow elastomeric sphere or making an utter fool of yourself prancing and screaming behind a plastic guitar?) [These images don't fit] my self-image either, but that's where the money is.

In truth, many engineers have done very well financially, but it was only at the price of moving up into an executive position. (See John DeLorean's On a Clear Day You Can See General Motors.) Would it be fair for the engineers to allow mankind to slide back into its primordial slime? Perhaps not.

The consuming public doesn't know what we do. They don't even care, as long as they can purchase the fruits of our intelligence—even our genius, for peanuts.

The fault, dear Brutus, is not in our stars, but in ourselves, that we are underlings.

Bill Taylor Lockheed Space Operations Orlando, FL

YOUR TURN

EDN's Signals and Noise column provides a forum for readers to express their opinions on issues raised in the magazine's articles or on any topic that affects the engineering industry. Send your letters to the Signals and Noise Editor, 275 Washington St, Newton, MA 02158. We welcome all comments, pro or con. All letters must be signed, but we will withhold your name upon request. We reserve the right to edit letters for space and clarity.



The integrated SCC that increases system performance and cuts CPU overhead in half. *Any* CPU.

The CMOS Integrated Serial Communications Controller (Z16C35 ") adds another level of performance and integration to Zilog's industry-standard SCC. And it'll work with whatever CPU you're using.

You cut real estate dramatically.

The ISCC's four DMA controllers (two per SCC channel) can cut your bus overhead by 50%, compared to industry-standard controllers. The maximum bus bandwidth of 3.1 Mbytes/second reduces both bus utilization and CPU overhead.

The continuing evolution of the SCC family.

Zilog's Superintegration" technology bas resulted in a rapidly growing library of working CPU and peripheral cores and cells that have been combined and enhanced for specific applications. And all of them use the same proven architectures and instruction sets you're already working with. For communications applications, specifically, we've developed fast-growing SCC and USC families that provide the extra speed and performance you need without overloading the CPU.

Within the SCC family of general purpose controllers there's a constantly developing line of progress toward even higher levels of integration. The industry-standard SCC, and now, the ISCC make that point clearly.

And just as clearly, they're just the beginning. The exciting "smart" SCC will take the process one important step further.

Since you've got a programmable bus interface, there's no need for programmable array logic on board. Plus you've got a more compact code to work with.

You pick the CPU.

The new streamlined, general purpose bus architecture is programmable in 8- or 16-bit data widths and 8-, 16- and 32-bit address bus widths. The ISCC's bus architecture is programmable to accept multiplexed or non-multiplexed formats.

You improve system performance.

Available in 10, 12.5 and 16 MHz versions, the ISCC will give you a data transfer rate of up to 4 Mbit/sec. You've also got a 10 x 19 bit status FIFO and a 14-bit byte counter for high speed SDLC transfer, using on-chip DMA controllers. Besides the low power CMOS and Superintegration™ advantages, you have performance enhancers like on-chip baud-rate generators, digital phased locked loops and crystal oscillators. And the ISCC supports all the current SCC features, including multiprotocol operation.

You choose.

The ISCC is designed for applications that don't require the higher bit rates of the USC, but do require DMA interface to larger memory systems as found in networked small computers, for example. In fact, it's the only integrated general purpose alternative available. It's also off the shelf. And backed by Zilog's proven quality and reliability. To find out more about the ISCC or any of Zilog's rapidly growing family of Superintegration products, contact your local Zilog sales office or your authorized distributor today. Zilog, Inc., 210 Hacienda Ave., Campbell, CA 95008, (408) 370-8000.

Right product. Right price. Right away.



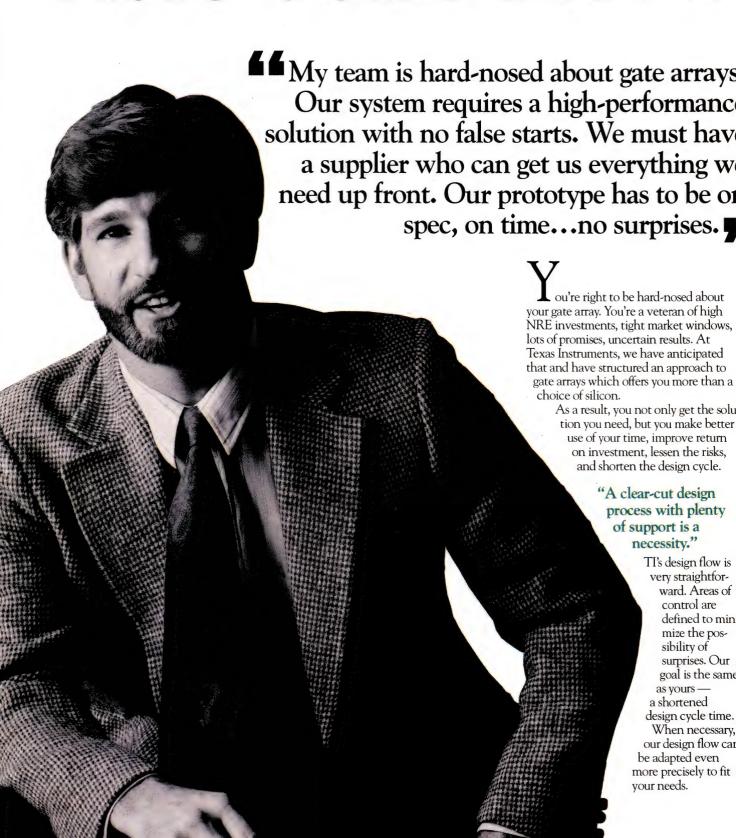
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EDN March 1, 1990 CIRCLE NO. 45

IN THE ERA OF MegaChip™ TECHNOLOGIES

ASIC SOLUTIONS



GATE ARRAYS

Tl's service and support are comprehensive — and available to you from Texas to Taiwan. Among the highlights:

Our TGC100 Series Design Kit, operating on Daisy/Cadnetix (DAZIX™), Mentor Graphics™, and Valid™ workstations, provides the necessary information to easily implement your gate-array design.

Person-to-person advice and counsel are provided worldwide by ASIC applications specialists in our field sales offices. ASIC design specialists are stationed at ASIC design centers in our Regional Technology Centers, where our design workshop is also conducted regularly.

Delivery schedules can be tailored to support your ship-to-stock or just-in-time programs anywhere in the world.

"We demand high performance in our arrays."

The TGC100 arrays are fabricated in TI's l-micron EPIC™ CMOS process technology. Typical gate delays are 500 ps with flip-flop toggle rates up to 208 MHz.

"We prefer a choice of densities plus design options."

plus design options."
TI's TGC100 arrays range in complexity up to 26K gates. You call the shots on pin count, pinout definition, and the package itself by choosing from our variety of pack-

ages having pin counts up to 256 pins (see table below).

TI's gate-array library contains more than 200 macros, many essential to attaining high-performance designs. For example, a clock distribution macro minimizes clock skew. Input/output buffer macros minimize unwanted voltage transients and drive heavy capacitive loads.

In support of the JTAG standard, SCOPE™ macros permit incorporation of design-for-test features.

A path-length criticality parameter allows you to specify the delays on critical nets. This acts to minimize the physical length of the interconnect traces and reduce overall propagation delay.

When you have more demanding requirements, the following options give you maximum flexibility in achieving the exact gate array you need:

- Additional prototypes
- Additional l-MHz test vectors
- \bullet Prototype devices tested over temperature and V_{CC} ranges plus DC parametrics
- Critical-path delay measurements (pin-to-pin)
- "At speed" test vectors
- Nonstandard V_{CC} and ground-pin locations
- Operating temperature range other than 0°C to 70°C

Tomorrow's outlook

Just as our TGC100 Series gate arrays meet the majority of your needs today, our gate arrays of tomorrow will fill the predominant industry needs for submicron densities.

Already, TI has disclosed an array having 106K gates, fabricated with TI's EPIC-II, 0.8-micron BiCMOS technology. High density combines with high performance — ECL speeds at CMOS power levels. This technology is the foundation for an entire family of submicron ASIC products from TI.

For more information on TI gate arrays, call, fax, or write us. In Europe call 44-234-223000, fax 44-234-223459, or write Customer Response Centre, MS 09, Texas Instruments Limited, Manton Lane, Bedford MK41 7PA, England. In Japan call 81-3-769-8700, fax 81-3-457-6777, or write Texas Instruments Japan Limited, MS Shibaura Building 9F, 4-13-23 Shibaura, Minato-Ku, Tokyo 108, Japan. In Hong Kong call 852-735-1223, fax 852-735-4954, or write Texas Instruments Hong Kong Limited, Market Communications Department, 8th Floor World Shipping Centre, 7 Canton Road, Kowloon, Hong Kong.

TI'S TGC100 SERIES COMMERCIAL GATE ARRAYS

											PROD	DUCTIO	ON PA	CKAGI	OPT	ONS													
GATE- ARRAY TOTAL MAX		MAXIMUM			PLASTIC DIP		PLASTIC LEADED CHIP CARRIER			PLASTIC PLASTIC QUAD-FLAT PACKAGE* PIN-GRID ARRAY																			
TYPE	CELLS	USABLE (90%)	PADS	28	40	28	44	68	84	80	100	120	132	144	160	208	240	100	120	132	144	180	208	256					
TGC104	3,600	3,240	100	х	V	V	V	v	V		1.0							Y						25					
TGC105A	4,500	4,050	100	^	^	^	_ ^	1^	1.^									^						1					
TGC106	5,600	5,040	130	V	v		V	V	V		10		_					Y	Y	Y									
TGC107	6,720	6,048	130	^	^		1^	^	1^		انتاا		T						_^	_^									
TGC108A	8,340	7,506	158	V	V		V	V	V		1.0							Х	Y	Y	Y	Х		100					
TGC110	10,008	9,007	. 130	° .	^	^	^ !			^	^	^									^	. ^	^	_^_	^		3.0		
TGC113	12,654	11,389	196					v	V				_					Х	Y	Y	Y	Y	Y						
TGC115A	14,706	13,235	190										. ^					Т					_^	^	^.	^	^	^	1
TGC116	15,580	14,022	216										_							Y	Y	Y	Y	V					
TGC119	18,620	16,758	210	210																	^	^	^	^	^				
TGC122	21,854	19,669	256																			\ \	V	V					
TGC126	25,868	23,281	ಬಂ	alvási	Service.	naro. 113	38 . 60	and the same	Marie C	The said	eti seri	The Carlo	in an air	1.00 mg/s/2	Medic	9100		No.	20,006	5.75	188			^					

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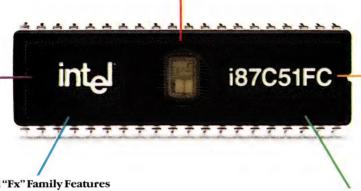
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AND/OR combination

of events. Qualification by

number of occurrences.

Conditional on

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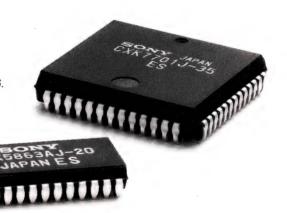
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FAST CACHE.

Cache memory for Intel 80386. Also standard SRAM line down to 8K x 8 @ 20 ns. 16K x 4 @ 15 ns.



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Ultra-high speed cache.

MODEL

CXK7701J*

CXK5863AP

CXK5863AJ

CXK5466P

CXK5466J

CXK5467P**

CXK5467J**

*For Intel 80386

CONFIG.

8K x 16

8K x 8

8K x 8

16K x 4

16K x 4

16K x 4

16K x 4

**0/E

15/20

15/20

15/20

Via a unique 0.8-micron

process, Sony covers your fast processor cache-memory needs two distinct ways.

First, there's our Model CXK77011. designed specifically for the Intel 80386.

This application-specific memory (ASM) combines address latch, memory and transceiver within one IC. Ready for user

configuration **ULTRA-HIGH SPEED CACHE SRAMS** as either an SPEED (ns) PACKAGE 8k x 16-bit 30/35/45/55 PLCC memory or 20/25/35 DIP 300 mil as two 4k x 16-20/25/35 SOJ 300 mil bit memories. 15/20 DIP 300 mil

SOJ 300 mil

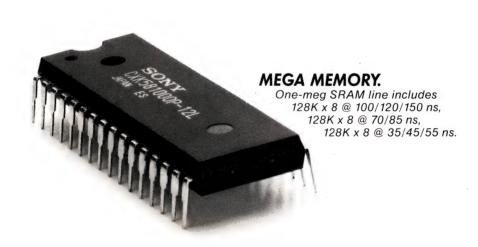
DIP 300 mil

SOJ 300 mil

Second. consider our new ultra-high speed SRAM capabilities.

As you scan the chart above keep in mind even higher speeds will be available soon.

TS SRA HE EXTREMES.



Ultra-high density.

Sony solves your board-space problems with three new 1-Mbit

MODEL

CXK581000P

CXK581000M

CXK581001P

CXK581001 M

CXK581020SP

CXK581020J

SRAMs.

Each is based on our 0.8-micron CMOS technology. Configured as 128K x 8 bits. And available in 32-pin DIP and

surface-mount plastic packages. And not only do Sony 1-Mbit

SRAMs maximize board space, but process speeds as well.

Nowhere else will you find a greater choice: 100/120/150-ns, 70/85-ns and 35/45/55-ns speed

PACKAGE

DIP 600 mil

SOP 525 mil

DIP 600 mil

SOP 525 mil

DIP 400 mil

SOJ 400 mil

HIGH-DENSITY SRAMS

SPEED (ns)

100/120/150

100/120/150

70/85

70/85

35/45/55

35/45/55

CONFIG.

128K x 8

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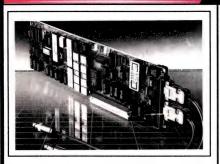
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1992 and the EEC Directive on EMC (short course), Orlando, FL. Interference Control Technologies, Box D, Gainesville, VA 22065. (703) 347-0030. March 6 to 8.

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The International Congress on Optical Science and Engineering/Exhibit, The Hague, The Netherlands. The International Society for Optical Engineering, Box 10, Bellingham, WA 98227. (206) 676-3290. FAX 206-647-1445. March 12 to 16.

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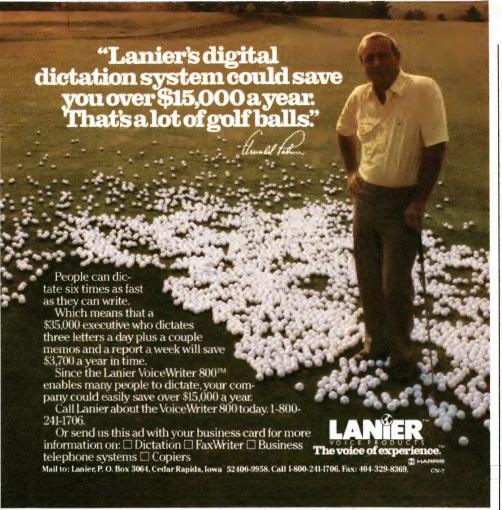
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Advances in Semiconductors and Superconductors: Physics Toward Device Application and Exhibit, San Diego, CA. The International Society for Optical Engineering, Box 10, Bellingham, WA 98227. (206) 676-3290. FAX 206-647-1445. March 17 to 21.

Professional Development Seminar, Houston, TX. USENIX Association, 5398 Manhattan Circle, Boulder, CO 80303. (303) 499-2600. FAX (303) 499-2608. March 19.

Second Annual Oregon Workshop on Software Metrics, Portland, OR. Warren Harrison, The Oregon Center for Advanced Technology Education, Portland State University, Portland, OR 97207. (503) 725-3108. FAX 503-725-4882. March 19 to 20.

NCGA '90—Conference and Exposition, Anaheim, CA. NCGA '90, National Computer Graphics Association, 2722 Merrilee Dr, Suite 200, Fairfax, VA 22031. (800) 225-6242; in VA, (703) 698-9600. FAX 703-560-2752. March 19 to 22.

CASE World Conference/Exposition, Los Angeles, CA. Digital Consulting Inc, 6 Windsor St, Andover, MA 01810. (508) 475-6990. March 20 to 22.

Mid-Lantic Electronics Show '90, King of Prussia, PA. Judith Ginsberg, Electronic Representatives Association, Mid-Lantic Chapter, 4113 Barbery Dr, Lafayette Hill, PA 19444. (215) 828-2271. FAX 215-941-6773. March 20 to 22.

Flat Panel Displays—New Technology Developments and Emerging End-Use Applications, Boston, MA. Frost & Sullivan Inc, 106 Fulton St, New York, NY 10028. (212) 233-1080. FAX 212-619-0831. March 26 to 27.

EDITORIAL

Let's recognize innovations







Jesse H Neal Editorial Achievement Awards 1987, 1981 (2), 1978 (2), 1977, 1976, 1975 American Society of

Business Press Editors Award

1988, 1983, 1981

Our editors look at many new products, but we can publish information for only a few of those products in each issue. On occasion, one or two new products show a great deal of innovation, and we think they deserve special recognition. So as part of our continuing program to highlight and recognize innovation, we will carefully select and publicize innovative products that rate your attention. You'll find the innovative products—when we write about them—on the new EDN Editors' Choice page in our Product Update section.

We realize that most of the products we don't select for the Editors' Choice page are still well designed and useful, and that they'll help you do a better design job. You need power supplies that are smaller, ICs that are faster, and computers that are more powerful, but not all of these new products are innovative.

Running our Editors' Choice program means we're taking a chance. The companies whose products we choose will love us; the others may hate us. But we're not concerned about being controversial as long as we serve your need for information and as long as we are fair judges. We're going to be very selective, though. In fact, we may skip an issue or two if we don't find a product that meets our standards for innovation.

Our selections might seem biased unless you know the rules, too. So, here are the criteria we'll apply: If it's an innovative product,

It offers significantly higher levels of performance in ways not previously available.

It solves a continuing problem much more effectively than its predecessor—if any.

It exhibits a marked degree of "cleverness," which differentiates it from earlier products.

It embodies new technology that advances the state of the art, or it uses older technology in a unique and innovative way. It might not have an immediate, widespread, or obvious use. Some innovative products take time to catch on and fire the imagination of designers.

And one final rule—the judges' selections are final.

We'll consider *all* of the products that we normally receive information about for the Editors' Choice page, so there's no need to send us a special innovation entry. However, if you have a new product that is particularly innovative and we haven't seen it before, do tell us about it. We want to recognize more innovations.

Jon Titus Editor

Be Brilliant At In Production



7:05 am : Breakfast

Suddenly, between bites, the answer to that new system design jumps right into your brain. But how to make it work in silicon? Use an Actel field programmable gate array!



8:50 am: Design

You warm up the design program on your 386 and put in the final touches. Then a quick rule check and 25 MHz system simulation with the Action Logic System software.



11:00 am: Place & Route

You watch the system place and route all 1700 gates (out of 2000 available) in under 40 minutes. 100% automatically! A final timing check. Then think of something to do until lunch.



12:00 pm : Lunch

Remember lunch? Normal people actually stop working and have a nice meal — right in the middle of the day! With Actel's logic solution, this could become a habit.

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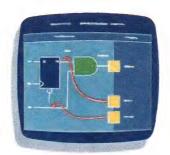
And do it in hours instead of weeks. Even between meals.

How? With features like 85% gate utilization. Guaranteed. Plus 100% automatic

Breakfast And v Dinner.

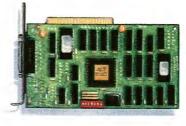


1:15 pm: Program You load the Activator™ programming module with a 2000-gate ACT 1020 chip and hit "configure" Take a very quick coffee break while your design becomes a reality.



1:25 pm : Test You do a complete, real-time performance check, with built-in test circuits that provide 100% observability of all on-chip functions. Without

generating any test vectors.



4:00 pm: Production Your pride and joy is designed, created, tested, and

off to the boys in Production. And you're finished way ahead of schedule! Better think of something to do until 5:00.



6:00 pm: Dinner

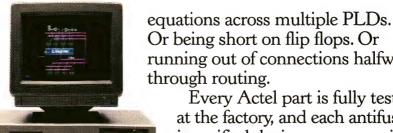
Remember dinner? Normal people actually go home and eat with their families. On your way, start thinking about how Actel's logic solution can help you be brilliant tomorrow.

placement and routing. Guaranteed. So you finish fast, and never get stuck doing the most tedious part of the job by hand. And design verification is quick and easy, with on-chip Actionprobes[™]

that work with your logic analyzer to provide 100% observability

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SELECTION GUIDE

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	AD202/AD204	AD208	AD210	AD203
Description	Low Cost Isolator ¹	Precision Isolator ¹	3-Port Isolator ¹	Rugged MIL Temp Isolator ¹
Isolation Voltage (V pk)	±1000 and ±2000	±1000 and ±2000	±3500	±2000
Nonlinearity (%)	±0.025 and ±0.05	±0.015 and ±0.03	±0.012 and ±0.025	±0.025
Gain Range (V/V)	1-100	1-1000	1-100	1–100
Bandwidth (kHz)	2 (AD202) 5 (AD204)	4	20	10 - ৬-০ুটুৰ্
Comments	SIP & DIP Packages	1.5 μV/°C Max Offset (RTI) Drift	High CMV Rating	Rated over -55°C to +125°C

NOTES

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Description

Isolation Voltage (V pk) Nonlinearity (%)

Input Range

Output Range

Comments

ANALOG DEVICES

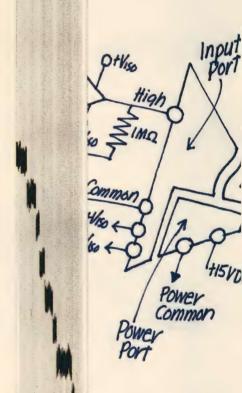
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±0.02	±0.02	±0.10 ²	±0.035
0–10 V	0-10 V 0-5 V	20 Ω to 5 kΩ	±10 mV to ±5 V
0–20 mA or 4–20 mA	0-20 mA or 4-20 mA	±10 V	±10 V
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KEITHLEY INSTRUMENTS

TECHNOLOGY UPDATE

ROM emulation reaches far-flung fields



ROM emulation is a key that will open more than one door.

Charles H Small, Senior Editor here's far more to ROM emulation than the name suggests. Certainly, as Table 1 shows, you can still get plenty of simple, inexpensive ROM emulators. But the technique of ROM emulation is popping up in unexpected areas such as PROM programming, incremental compilers, μ P-system in-circuit emulation, and logic analysis.

The ROM emulators in Table 1 require little detailed explanation. The simplest draw their power from the target system and get their data in predigested form from a custom program running on an IBM PC. Others are self powered and can accept common formats like Intel Hex and Motorola S records. Some only accept data files, and others have enough smarts to execute simple

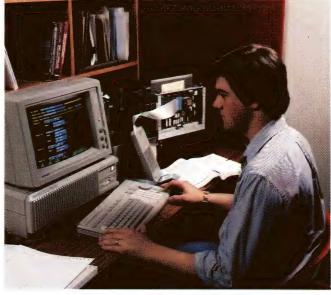
memory-debugging commands.

Be careful when dealing with self-powered ROM emulators. Make sure that you investigate just what their behavior is when you power-down your target system. Note also that generally, you must pay a premium to get the fastest version of a given ROM emulator.

Although a μP emulator gives you greater control over your target system than a ROM emulator does, ROM emulation has a couple of advantages over μP emulation. First, μPs are more often soldered in; EPROMS

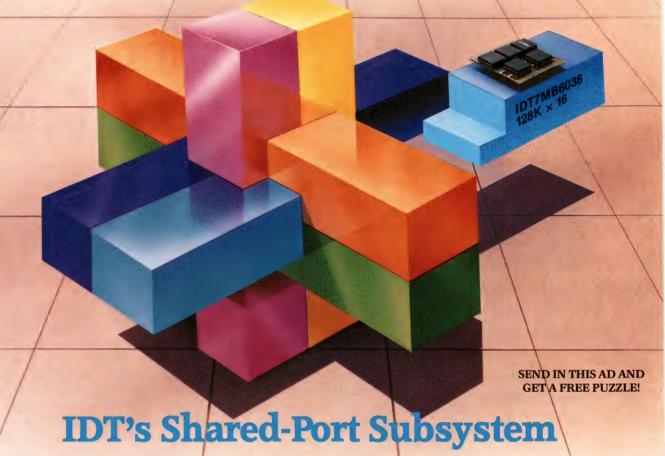
use sockets. Thus a ROM emulator is often more practical than a μP emulator. Also, ROM emulators are much less expensive than μP emulators because they are much simpler to emulate. The utility of the ROM emulators in **Table 1** is easy to appreciate for anyone who has ever done "blow-and-go" software development using EPROMs.

If your target system's programs execute out of EPROM, developing software involves a tedious and error-prone cycle. Ceaselessly, you assemble your code, download it to a PROM burner, burn the code into an EPROM, and then plug the EPROM into your target system to begin debugging. If your program does have a bug, you must unplug the EPROM, erase it, and start the cycle over again.



When tightly coupled with other elements, a ROM emulator gives the Prism 3000 logic analyzer from Tektronix control over a target system.

Putting It All Together



Here's the Puzzle

How do you build a flexible, expandable, low cost shared memory with two independent ports that is guaranteed to work without having to design, manufacture, test, debug, and burn-in an assortment of individual components? Look to IDT's Shared-Port subsystem, part of IDT's family of "Building Blocks for the '90s".

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TECHNOLOGY UPDATE

ROM emulation

A ROM emulator prunes this cycle because you can directly download your program from your host computer into the ROM emulator and begin debugging immediately. The key feature of the ROM emulator is that it is a form of dual-port memory: one port hooks to your host computer, and the other port hooks to your target system.

A different path

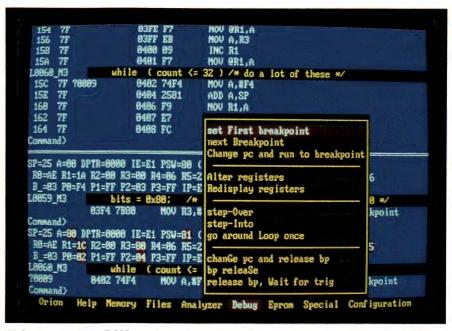
Thus a ROM emulator, much like the more common μP -emulator, is inherently an entry path into your target system that is independent of any designed-in paths, such as serial and parallel ports. Designers are using this independent path into a target system in a variety of ways.

For example, Stag Microsystems's PP39 EPROM programmer can dump your program into the company's \$495 stand-alone model E100 EPROM emulator instead of an EPROM. Programming a 512k-bit EPROM can take several minutes—erasing it takes 20 minutes. With the company's ROM emulator substituting for an EPROM device, downloading a program takes only 10 sec.

The company also bundles the ROM emulator with an IBM PC interface card and a software-development package for \$1795. The package includes a symbolic debugger that works with an emulator-resident debugging monitor via your target system's serial line.

Compiler target

Forth-Systeme bundles its Time-1 ROM emulator (DM2500) with its version of Laboratory Microsystems Forth programming environment (DM5000). With this package, you can write Forth programs on your IBM PC that compile directly, in one step, into the memory space of your target system. This hardware/software combination reduces



With extensions, a ROM emulator, such as this one from Orion Instruments, can be a μP -system in-circuit emulator.

the steps between writing code and trying it out to an absolute minimum; none.

Forth, being an incremental compiler, makes this reduction in steps possible. Each time you define a new Forth word (equivalent to writing a line of code in other languages), the Forth compiler immediately adds that word to its "dictionary" (object module). The compiler adds the line without any of the steps that other, less sophisticated languages necessitate such as compiling, assembling, linking, locating, and loading.

Expanding ROM emulation into the areas of in-circuit emulation and logic analysis involves two additions to the basic concept. The first is setting up 2-way, rather than just 1-way, communication between the host computer and the target system's μP ; the second is putting some resident, system-development code into the emulation memory.

The latter is child's play. After all, storing code is what a ROM emulator does. However, you must be aware of the presence of this ad-

ditional parasitic code and allow for its effects.

Establishing 2-way communication is a little trickier. Because most designers don't connect write-enable circuitry to their EPROMS, the target μP cannot simply write messages to the emulation memory. Nor does merely controlling the target system's EPROM give you absolute power over its μP and peripherals.

The most common scheme for allowing the ROM emulator to control the target system's μP involve letting the ROM emulator take over the μP 's interrupt (NMI) pin.

For example, even B&C Microsystems's simple \$395 RomEm ROM emulator has a word recognizer monitoring the EPROM's address bus. This word recognizer has trigger-in and trigger-out lines. You can connect the word recognizer's trigger-out line to the target system's NMI pin to halt the μ P when your program accesses a preset address. Once an instrument designer includes these two additions, the ROM emulator can function, for

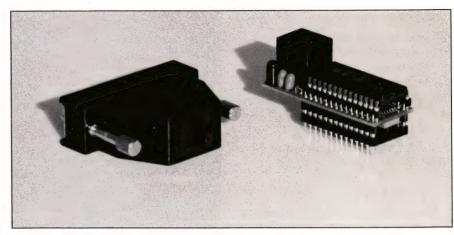
TECHNOLOGY UPDATE

ROM emulation

example, as a microsystem in-circuit emulator.

Orion Instruments' \$4980 8620 incircuit emulator supports over 170 µPs and variants with \$660 to \$1050 personality adapters. The instrument differs from the simple ROM emulators in **Table 1** in three respects: you can partition its 128k-byte ROM-emulation memory in 2k-byte segments; it has a 48-channel bus-state analyzer; and it has a built-in EPROM burner/reader. The unit's software includes a target-system-resident debugging monitor and a high-level-language debugger for your host IBM PC.

In addition to the resident debugger's ROM space, the unit requires a few bytes of RAM and control of the target μP 's NMI pin. With this control, the unit can effect single-stepping, breakpoints, and μP access. You can cross-trigger the emulation memory and the instrument's bus-state analyzer.



So small that the entire device can plug directly into the target system, the ROM emulator from Parallax communicates with a host IBM PC by means of a modular telephone cable.

Similarly, Z-World's \$595 ICE-PROM is a ROM emulator that functions as a microsystem in-circuit emulator for Z80 family processors (HD64180, Z180, and NSC 800). Like Orion's emulator, Z-World's emulator requires a memory-resident debugger.

However, the target-system's μP

communicates with the host computer in a novel manner. The ROM emulator reserves a 512-byte page of memory. The ROM emulator's control circuitry interprets reads by the target system's μP to various defined addresses in this so-called "hot page" as messages from the target system.

Manufacturer	Model	Price (\$)	Emulation memory size (× 8k bits)		gable 32-bit wide	Self- powered	Power-down protection	Battery- backed	Host interface	Minimum access time (nsec)	Comments
Applied Data Systems	DPROM-32k DPROM-64k	195 245	32 64	Yes Yes	Yes Yes	No No		NiCd NiCd	Serial Serial	100 100	
B&C Microsystems	Rom Em	395	64	Yes	Yes	Yes		NiCd	Parallel	100	
Future Systems	EE-100	995	64			Yes	Yes		Serial	150	
GTEK	ROMX-2 ROMX-2L	399 499 to 999	32 128	Yes Yes	Yes Yes	Yes Yes		Li Li	Serial Serial	85 85	Halt line
Grammar Engine	PROMICE	1695	512	Yes	Yes	Yes	Yes		Serial	150 std	Can access emulation memory while target system is running.
Macrochip Research	Memulator 16 Memulator 512 Memulator 1023 Memulator 1024 Memulator II	995 475 795 795 375	32 64 128 64 32	Yes		No No No No		Yes Yes Yes	Serial Serial Serial Serial Serial	50 100 100 100 50	Memulator 16 is dual-chip emulator. All units have ex ternal write lines.
Micro Computer Control	Micro/Emmy-32k Micro/Emmy-64k	195 295	32 64			No			Serial	130	
Parallax	2764 ROM Emulator	129 (RAM \$20)	8			No			Serial	120	Entire emulator plug into target's socket.

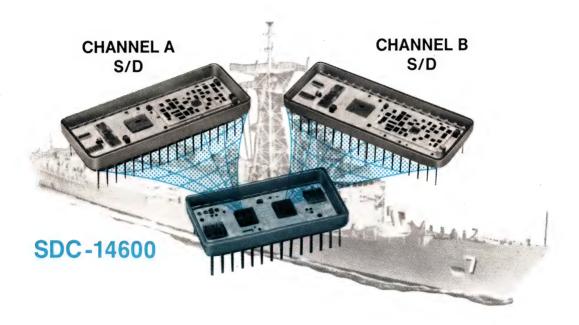


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For more information or applications assistance, call Bill Cullum at 516-563-5678 or contact the DDC office nearest you.

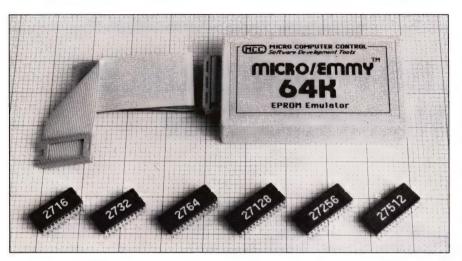
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TECHNOLOGY UPDATE

ROM emulation



Because all EPROMs are pretty much alike, Micro Computer Control's ROM emulator can substitute for a range of EPROM devices.

Tektronix included ROM emulation in its Prism 3000 modular logic analyzer. Feeling that a meaningless name would be less confusing than the name ROM emulator, Tek calls its ROM emulator a PDT (prototype debug tool). The logic analyzer's high-speed bus tightly couples this ROM emulator with other elements in the analyzer.

Also, the logic analyzer's control circuitry can write to the dual-port ROM emulator between the target system's memory-access cycles; most other ROM emulators allow either the target system or the host computer to access emulation memory but not both simultaneously.

Thus in conjunction with an emulation-memory-resident 256-byte debugging monitor, the modular logic analyzer can control and monitor a target system's high-speed events, microbus transactions, and software performance in real time. Tek quotes a "base" price of \$8400 for the analyzer.

Article Interest Quotient (Circle One) High 518 Medium 519 Low 520

For more information . . .

For more information on the ROM emulators discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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B&C Microsystems Inc 335 W Olive Ave Sunnyvale, CA 94086 (408) 730-5511 Circle No. 701

Forth-Systeme Angelika Flesch Box 1103 D-7814 Breisach West Germany (49) 7667-551 FAX (49) 7667-555 Circle No. 702

Future Systems Inc 21634 Lassen St Chatsworth, CA 91311 (919) 407-1647 FAX 818-407-0681 Circle No. 703 Grammar Engine 3314 Morse Rd Columbus, OH 43231 (614) 471-1118 Circle No. 704

Gtek Inc PO Box 2310 399 Highway 90 Bay St Louis, MS 39521-2310 (601) 467-8048 FAX 601-467-0935 Circle No. 705

Macrochip Research Inc 1301 N Denton Dr, Ste 204 Carrollton, TX 75006 (212) 242-0450 FAX 214-245-1005 Circle No. 706

Micro Computer Control Corp Box 275 Hopewell, NJ 08525 (609) 466-1751 FAX 609-466-4116 TWX 910-240-4881 Circle No. 707 Orion Instruments Inc 702 Marshall St Redwood City, CA 94063 (415) 361-8883 FAX 415-361-8970 TLX 530942 Circle No. 708

Parallax Inc 6200 Desimone Ln, #69A Citrus Heights, CA 95621 (916) 721-8217 Circle No. 709

Stag Microsystems Inc 7524-B Swans Run Rd Charlotte, NC 28226 (704) 541-8282 FAX (704) 541-8600 Circle No. 710 Tektronix Inc Logic Analyzer Div Box 12132 Portland, OR 97212 (800) 245-2036 Circle No. 711

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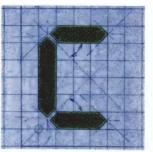
processing speeds, two

or more RTX chips an be tied together

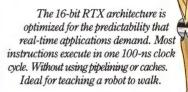
for parallel processing, as in this

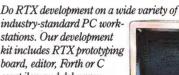


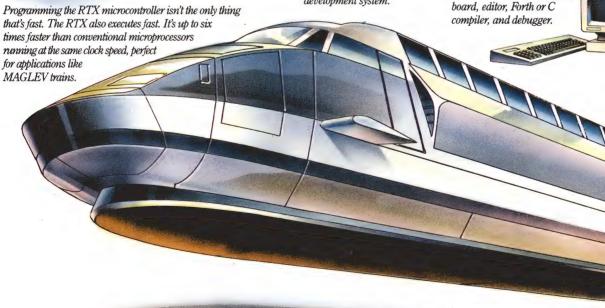
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TECHNOLOGY UPDATE

4-BIT MICROCONTROLLERS

ICs combine \(\mu Ps \) with myriad I/O options



Manufacturers continue to broaden their lines of 4-bit microcontrollers, offering many with specialized functions. Several years will pass before as many 8-bit µCs become available, but chances are you'll never need 8 bits or more.

Maury Wright, Regional Editor

oday's 4-bit microcontrollers (μCs) offer almost unlimited combinations of core processors, memories, I/O functions, packaging, and operating characteristics. In addition to the wide variety of chips available, many devices also provide specialized functions such as phone dialers and television tuners. Other common features in 4-bit µCs include A/D and D/A converters and LED and LCD drivers. Also, manufacturers now offer the ICs in onetime-programmable and EEPROM versions and with supply-voltage requirements as low as 2V. Because of the abundance and diversity of 4-bit µCs, you're almost guaranteed to find a device that suits your design.

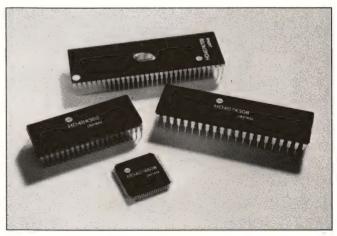
Table 1 reveals many of the 4-bit μ Cs available, including numerous specialized versions. If you don't see what you're looking for, call a manufacturer; the manufacturers all offer customization in appropriate quantities. In addi-

tion, the companies plan to add to their product lines, and they often do so in cooperation with a strategic customer.

The 4-bit chips meet the price and performance requirements of a variety of consumer applications, such as homeelectronic applications in telephones, televisions, and stereos. Other typical consumer applications include dishwashers, automobile instrumentation, and exercise equipment. Customers usually purchase 4-bit microcontrollers in volumes of 10,000, 100,000, or more. In such volumes, the ICs range in cost from less than \$0.50 for certain NMOS devices from National Semiconductor to \$5 or more for chips with specialized functions such as television tuners or EEPROMs. Most of the 4-bit devices in the **table** cost from \$1 to \$2.

For most designers considering a 4-bit device, performance takes a back seat to other systems issues such as cost, voltage and power requirements, and integrated functions. Still, you must consider the performance a device offers and remember that instructions are 4 bits in length.

Recent devices, such as the HMCS412/414/424 from Hitachi, offer instruction cycles of less than 1 µsec. However, Hitachi also offers a number of devices that have a 20-µsec cycle. To improve performance, the Hitachi devices employ a 10-bit instruction



The availability of many packages illustrates the wide variety of 4-bit μ Cs offered by Hitachi. The company's 4-bit devices offer many options in memory and I/O configurations.

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Since the FS700 receives the ground wave from the LORAN transmitter, reception is unaffected by atmospheric changes, with no possibility of missing cycles, common occurrence with WWV due to discontinuous changes in the position of the ionosphere layer. Cesium and rubidium standards, in addition to being expensive in tially, require periodic refurbishment, another costly item

The FS700 system includes a remote active 8-foo whip antenna, capable of driving up to 1000 feet of cable. The receiver contains six adjustable notch filters and a frequency output which may be set from 0.01 Hz to 10 MHz in a 1-2-5 sequence. A Phase detector is used to measure the phase shift between this output and another front panel input, allowing quick calibration of other timebases. A analog output with a range of \pm 360 degrees, provides voltage proportional to this phase difference for driving strip chart recorders, thus permitting continuous mon toring of long-term frequency stability or phase locking cother sources.



FS700: The optimum frequency management systen

TECHNOLOGY UPDATE

4-bit microcontrollers

bus and 10-bit-wide ROMs inside the chip. Most available devices have cycle times between 1 and 10 usec.

A fast instruction cycle often means a sacrifice in other characteristics, such as power or temperature requirements. Certain Hitachi devices, for example, come in three versions: A 5V version may execute instructions in 10 µsec, a low-power 5V version may take 20 µsec, and a 3V device may require 20 µsec. Fujitsu offers a number of µCs that operate at 2.5V but that have an instruction cycle time of 7.5 µsec. Functionally identical 5V devices feature a 3-µsec cycle.

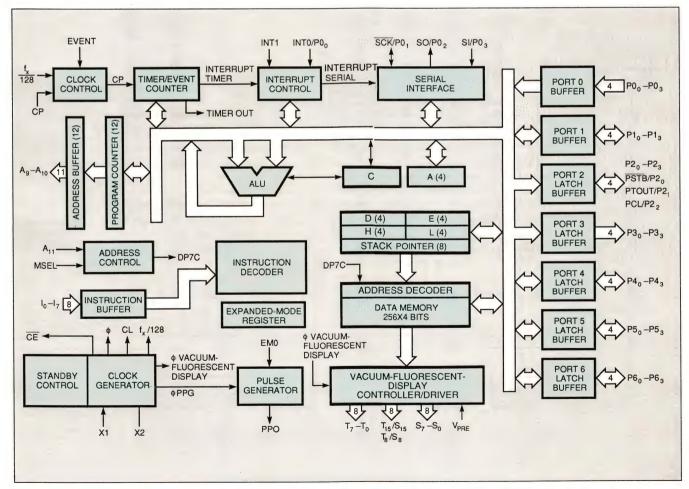
In 4-bit devices, a lower supply voltage is usually more important

than less power consumption. The chips suit many battery-powered applications and therefore need a low supply voltage. NEC and Toshiba offer 4-bit μ Cs with supply requirements as low as 2.2V. Almost all the 4-bit μ Cs in the **table** offer low-power or standby modes.

Memory configuration also plays a key role in choosing a 4-bit μC for your design. Except for certain devices targeted for development purposes, all of the microcontrollers in the **table** include some ROM and RAM on chip. Older devices have as little as 512 bytes of ROM, more recent ones feature as much as 8 or 16k bytes, and NEC plans to offer 32k-byte versions later this year. The chips typically include be-

tween 128 and 1k nibbles (4 bits) of RAM.

Traditionally, the manufacturers in the table have only offered 4-bit microcontrollers with mask-programmable ROM. Mask programming is only cost effective in large quantities of μ Cs (10,000 or more). Furthermore, the mask-programming step can require months of lead time. The companies all offer development chips with EPROM or external connections to EPROM, but such devices aren't cost effective or environmentally suited for most target applications. Therefore, designers have turned to other processor technologies for applications with low-volume production requirements.



The 24 high-voltage signals available on the NEC μ PD7519 can directly drive vacuum-fluorescent displays. The μ C operates from a 2.5V supply, and it includes two power-down modes and 4k bytes of ROM.

TECHNOLOGY UPDATE

4-bit microcontrollers

Now Toshiba, NEC, and Hitachi offer many of their 4-bit µCs in onetime-programmable packages. You can program a device in minutes. The one-time-programmable devices can simplify development, serve limited production runs, and fill in for mask-programmed parts during delays after a new design or a design update. A one-time-programmable version of a µC currently costs three times more than a regular μC, but you can expect this premium to drop as volumes increase. Compared with the cost of discrete alternatives, triple the price can still be a bargain for certain highly integrated µCs.

NEC and Hitachi also offer

EPROM versions of certain chips that are suitable for various target applications. National Semiconductor offers 4-bit μ Cs that feature post-metal programming. This feature lets the company program the ROM after final metalization, thus shortening lead times of mask-programmable parts to as little as a few weeks.

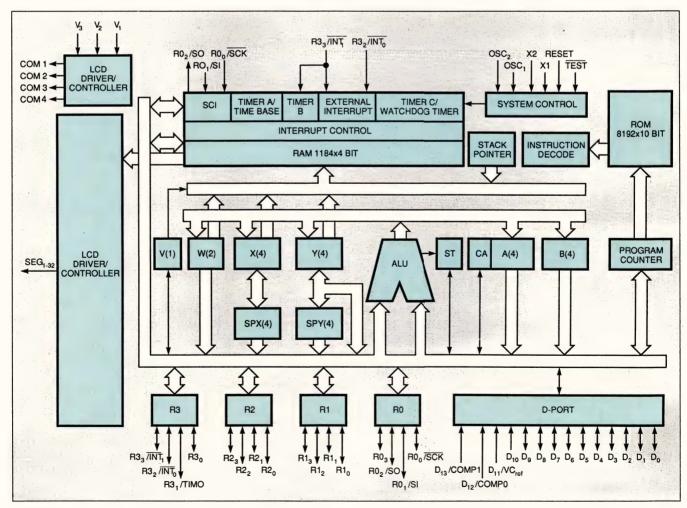
EEPROMs target security

EEPROM versions of certain 4-bit μ Cs will appear this year. To shiba has announced a handful of such devices and plans to ship them by midyear. Hitachi and NEC also plan to offer EEPROM versions. EEPROM-based μ Cs suit security

applications such as electronic locks and cable-television decoders.

If you think one of these 4-bit devices might be perfect for your next design project, rest easy about other development issues. You'll probably have to work in assembly language to program the chips, but because of its compact and efficient code, you'd most likely choose assembly language for such a project anyway.

All of the companies mentioned in this article offer IBM PC-compatible development software and hardware. To acquire the assemblers, debuggers, simulators, and emulators that you'll need, you can expect to spend between \$1500 and



The LCD driver/controller on the Hitachi HD404808 can drive a 16-digit display. The 4-bit μ C also includes an $8k \times 10$ -bit ROM array and a $1k \times 4$ -bit RAM array.

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TECHNOLOGY UPDATE

4-bit microcontrollers

\$10,000 (not including the cost of a PC). The low end of this price range buys support for a single device, and the higher prices usually buy support for a company's entire family of microcontrollers.

Assemblers support macros

All of the assemblers offered by the manufacturers for their μ Cs are state of the art; they include features such as macro capability and the ability to produce relocatable code. Toshiba also offers a PL/1-language compiler for its products. Because companies are offering versions of their μ Cs with bigger memories, you can expect to see Clanguage products available in the next year.

All of the manufacturers in the **table** expect 4-bit devices to continue their healthy growth. These companies offer 8-bit devices also, but not in as many flavors. The cost isn't holding them back from making more advanced 8-bit devices, however; in new process technolo-

gies, the incremental cost in silicon real estate, and therefore in dollars, to make an 8-bit core is small compared with the cost of manufacturing a 4-bit core. Nevertheless, it will take several years for the companies to broaden their 8-bit lines to the extent of 4-bit μ Cs. Furthermore, many applications don't require the processing power that 8-bit μ Cs offer, and they probably never will.

Table begins on pg 76

Article Interest Quotient (Circle One) High 512 Medium 513 Low 514

For more information . . .

For more information on the 4-bit- μ C products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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Hitachi America Ltd 2000 Sierra Point Pkwy Brisbane, CA 94005 (415) 589-8300 FAX 415-583-4207 Circle No. 714

National Semiconductor Corp Box 58090 Santa Clara, CA 95052 (408) 721-5000 TWX 910-339-9240 Circle No. 715 NEC Electronics Inc Box 7241 Mountain View, CA 94039 (415) 960-6000 TWX 910-379-6985 Circle No. 716

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DT1492-F	16SE	12	1, 2, 4, 8	150	2	130/DAC	16
DT1492-F	8DI	12	1, 2, 4, 8	150	2	130/DAC	16
DT1492-G	16SE	12	1, 2, 4, 8	250	2	130/DAC	16
DT1492-G	8DI	12	1, 2, 4, 8	250	2	130/DAC	16
DT1492-L	4DI	12	1	750	2	130/DAC	16
DT1495	16SE/8DI	12	1, 10, 100, 500	40/2.5	2	130/DAC	16
DT1497	4DI	16	1	100	2	130/DAC	16
DT1498	4SE(SS&H)	12	1	100	2	130/DAC	16

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Kong (5) 448963; India (2) 23-1040; Israel (52) 545685; Italy (2) 82470.1; Japan (3) 502-5550, (3) 348-8301, (3) 555-1111; Korea (2) 756-9954; Netherlands (7) 99-6360; New Zealand (64) 9-545313; Norway (2) 5312-50;
Portugal (1) 545313; Singapore (65) 779762; South Africa (12) 8037680/93; Spain (1) 455-812; Sweden (8) 761-7820; Switzerland (1) 723-3410; Tawan (2) 702-0405.

Table 1—Representative 4-bit microcontrollers

Manufac- turers	Model/series	ROM (bytes)	RAM (x4 bits)	I/O lines	cycle time (μsec)	voltage (V)	Temperature range (°C)	Package pins	Package type	Other features
Fujitsu	MB88200, H	512 to 1k	16 to 32	12	3, 1.5	3.5 to 6.5	-40 to +85	16	DIP,Q SOIC	10 to 12 LED drivers
	MB88200B	1k	32	23	3	5	-40 to +85	28	DIP	16 VFD drivers, 5 to 7 LED drivers
	MB88210	1k	32	10	3	5	0 to +70	20 to 24	DIP,Q SOIC	8-bit A/D converter, 10 LED drivers
	MB8850,F	1k to 2k	64 to 128	23 to 37	3 3 7.5	5 3.5 to 6.0 2.5 to 4.0	-40 to +85 -30 to +70 -30 to +70	28 to 48	DIP,SD, Q,SOIC	4-bit serial-port buffer, 8-bit counter
	MB8850B	2k	128	37	2	5	-30 to +70	42 to 48	DIP,SD, Q,SOIC	16 VFD drivers, 4-bit serial- port buffer, 8-bit counter
	MB8850H	2k	128	37	1.5	5	-40 to +85	42 to 48	DIP,SD, Q,SOIC	24 LED drivers, 4-bit serial- port buffer, 8-bit counter
	MB88500	2k to 4k	192 to 256	36	2.86 2.86 2.0	3.5 to 6.0 5 5	-30 to +70 -40 to +85 -40 to +85	42 to 48	DIP,SD, Q,SOIC	4- to 8-bit serial-port buffer
	MB88500H	2k to 4k	256	36	1.5	5	-40 to +85	42 to 48	DIP,SD, Q,SOIC	27 LED drivers, 4- to 8-bit serial-port buffer
	MB88510	4k	192 to 256	12 to 34	2	5	-40 to +85	28 to 48	DIP,SD, Q,SOIC	4- or 8-channel 8-bit A/D corverters, 30 LED drivers, 4- to 8-bit serial-port buffer, 8-bit counter
	MB88510B	4k to 8k	256	34 to 54	2	5	-40 to +85	42 to 64	DIP,SD, Q,SOIC	4- or 8-channel 8-bit A/D colverter, 15 to 25 VFD drivers, 19 to 28 LED drivers, 4- to 8-bit serial-port buffer, 8-bit counter
	MB88520	2k to 4k	256	57	2	5	-30 to +70	64	SD,Q SOIC	4- to 8-bit serial-port buffer, 8-bit counter
	MB88520B	4k	256	57	2	5	-30 to +70	64	SD,Q SOIC	24 VFD drivers, 4- to 8-bit serial-port buffer, 8-bit count
	MB88530	2k	128	32 to 34	3	5	-30 to +70	42 to 48	DIP,SD, Q,SOIC	3-channel 6-bit or 1-channe 13-bit D/A converter, 4-bit serial-port buffer, 8-bit count
	MB88540	4k	256	29 to 37	2	5	-40 to +85	80	Q,SOIC	24×4 to 32×4 LCD controlled driver, 4- to 8-bit serial-port buffer, 8-bit counter
	MB88550,H	6k to 8k	256	68	2, 1.5	5	-30 to +70	80	Q,SOIC	4-channel 5-bit A/D converte 4- to 8-bit serial-port buffer, 8-bit counter
	MB88560	3k to 6k	192 to 256	21	6.67	5	-40 to +85	80	Q,SOIC	3-channel 6-bit A/D converte 26×2 LCD controller/driver, 39 VFD drivers, AM/FM PLL 8-bit counter
	MB88570	5k	256	32	1.5	5	-40 to +85	42 to 48	DIP,SD, Q,SOIC	8-channel 8-bit A/D converte 4- to 8-bit serial-port buffer, 8-bit counter
Hitachi	HMCS44C,CL	2k×10	160	32	10, 20	5, 3	-20 to +75	42	DIP,SD	8-bit counter
	HMCS45C,CL	2k×10	160	44	10, 20	5, 3	-20 to +75	54 to 64	SD,F	8-bit counter
	HMCS46C,CL	4k×10	256	32	5, 20	5, 3	-20 to +75	42	DIP,SD	8-bit counter
	HMCS47C,CL	4k×10	256	44	5, 20	5, 3	-20 to +75	54 to 64	SD,F	8-bit counter
	LCD III	2k×10	160	32	10, 20	5, 3	-20 to +75	80	F	LCD drivers, 8-bit counter
	LCDIV	4k×10	256	32	4, 20	5, 3	-20 to +75	80	F	LCD drivers, 8-bit counter
	HMCS402AC,C,CL	2k×10	160	58	1.33, 2, 4	5, 5, 3	-20 to +75	64	SD,F	Serial port, two 8-bit counte
	HMCS404AC,C,CL	4k×10	256	58	1.33, 2, 4	5, 5, 3	-20 to +75	64	SD,F	Serial port, two 8-bit counte
	HMCS408AC,C,CL	8k×10	512	58	0.89, 2, 4	5, 5, 3	-20 to +75	64	SD,F	Serial port, two 8-bit counte

Key: DTMF = dual-tone multiple-frequency F = flatpack MF = miniflatpack

OPT = one-time-programmable PMP = post-metal programming

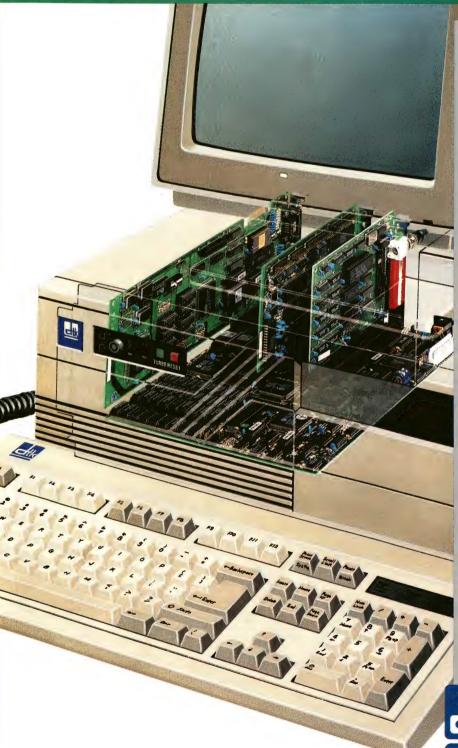
Q = quad flatpack

QI = quad in-line flatpack SD = shrink DIP

VFD = vacuum-fluorescent display

Table continued

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Table 1—Representative 4-bit microcontrollers (continued)

Manufac- turers	Model/series	ROM (bytes)	RAM (x4 bits)	I/O lines	cycle time (μsec)	voltage (V)	Temperature range (°C)		Package type	Other features
Hitachi	HMCS412AC,C,CL	2k×10	160	36	0.89, 2, 4	5, 5, 3	-20 to +75	42	DIP,SD	Serial port, two 8-bit counter
(contin- ued)	HMCS414AC,C,CL	4k×10	160	36	0.89, 2, 4	5, 5, 3	-20 to +75	42	DIP,SD	Serial port, two 8-bit counter
,	HMCS424AC,C,CL	4k×10	256	36	0.89, 2, 4	5, 5, 3	-20 to +75	42	DIP,SD	Serial port, two 8-bit counter
	HD4074008	8k×10	512	58	0.89	5	-20 to +75	64	DIP,SD,F	Serial port two 8-bit counters EPROM option
	HD4074308	8k×10	160	34	2	5	-20 to +75	42	DIP (4-channel 8-bit A/D converte tone generator, 26 high- voltage ports, two 8-bit counters, EPROM option
	HD4074408	8k×10	512	58	1	5	-20 to +75	64	DIP,SD,F	Two serial ports, two 8-bit counters. PWM output, EPROM option
	HD4074608	8k×10	1184	30	10, 5	5	-20 to +75	80	F	LCD controller/driver, DTMF generator, serial port, three 8-bit counters, EPROM option
	HD4074709	16k×10	512	56	. 1	5	-20 to +75	64	DIP,SD,F	VFD controller/driver, serial port, three 8-bit counters, EPROM option
	HD4074808	8k×10	1184	30	1	5	-20 to +75	80	F	LCD controller/driver, serial port, three 8-bit counters, EPROM option
	HD4074509	16k×10	512	29	1	5	-40 to +70	80	F. S	LCD controller/driver, PLL wi prescaler, 2-channel 8-bit A/D converter, two serial port two 8-bit counters, one 20-b counter
National Semicon-	COP410L,11L,13L,14L	512	32	15 to 19	16	5	-40 to +85	20 to 24	DIP,SOIC	NMOS, PMP option, serial port
ductor	COP410C,11C,13C	512	32	15 to 19	4	2.4 to 5.5	-40 to +85	20 to 24	DIP,SOIC	PMP option, serial port, military version available
	COP420,21,22	1k	64	15 to 23	4	5	-40 to +85	20 to 28	DIP,SOIC, PLCC	NMOS, serial port
	COP424C,25C,26C	1k	64	15 to 23	4	2.4 to 5.5	-40 to +85	20 to 28	DIP,SOIC, PLCC	PMP option, serial port, military version available
•	COP420L,21L,22L	1k	64	15 to 23	16	5	-40 to +85	20 to 28	DIP,SOIC, PLCC	NMOS, PMP option, serial port
	COP440,41,42	2k	160	19 to 36	4	5	-40 to +85	28 to 40	DIP	NMOS, zero-crossing detec circuit, serial port
	COP444C,45C	2k	128	19 to 23	4	2.4 to 5.5	-40 to +85	20 to 28	DIP,SOIC, PLCC	Serial port, military version available
	COP444L,45L	2k	128	19 to 23	15	5	-40 to +85	24 to 28	DIP	NMOS, PMP option, military version available
NEC	7501,02,03	1k to 4k	96 to 224	24	10	2.5 to 6	-10 to +70	64	MF	LCD controller/driver, serial port, 8-bit counter
	7514	4k	256	31	5	2.7 to 6	-10 to +70	80	MF	LCD controller/driver, serial port
	7507S	2k	128	20	5	2.2 to 6	-10 to +70	28	DIP,SD	Serial port, 8-bit counter
	7506,07,08	1k to 4k	64 to 224	22 to 32	5	2.5 to 6	-10 to +70	40 to 62	DIP,SD, MF	Serial port, 8-bit counter
	7507H,08H	2k to 4k	128 to 224	32	2.86	2.7 to 6	-10 to +70	40 to 44	DIP,SD	Serial port, 8-bit counter
	7508A	4k	208	32	5 to 10	2.7 to 5.5	-10 to +70	40	DIP	VFD drivers, serial port, 8-bi counter
	7554,64	1k	64	15 to 16	2.86 to 4	2.5 to 6	-10 to +70	20	SD,SOIC	LED drivers, serial port, 8-bi counter
	7556,66	1k	64	19 to 20	2.86 to 4	2.5 to 6	-10 to +70	24	SD,SOIC	LED drivers, 4-bit comparato 8-bit counter

Key: DTMF = dual-tone multiple-frequency

F = flatpack
MF = miniflatpack
OPT = one-time-programmable
PMP = post-metal programming

Q = quad flatpack QI = quad in-line flatpack SD = shrink DIP

VFD = vacuum-fluorescent display

Table continued



Table 1—Representative 4-bit microcontrollers (continued)

Manufac- turers	Model/series	ROM (bytes)	RAM (x4 bits)	I/O lines	cycle time (µsec)	voltage (V)	Temperature range (°C)	Package pins	Package type	Other features
NEC (contin-	7527A,28A,37A,38A	2k to 4k	128 to 160	35	3.3 to 5	2.7 to 6	-10 to +70	42	DIP,SD	VFD driver, serial port, 8-bit counter
ued)	7519,19H	4k	256	53	2.44 to 15.26	2.5 to 6	-10 to +70	64	SD,MF,QI	VFD controller/driver, serial port, 8-bit counter
	7516H	6k	256	53	2.44 to 15.26	2.5 to 6	-10 to +70	64	SD,QI	VFD controller/driver, serial port, 8-bit counter
	7533	4k	160	30	5 to 10	3 to 6	-10 to +70	42	DIP,SD, MF	4-channel 8-bit A/D converted serial port, 8-bit counter
Toshiba	TMP42C40P,60P, 50N,70N,70M	512 to 1k	32	11 to 23	1	.5	-40 to +85	16 to 28	DIP,SD, SOIC	
	TMP42C66P	1k	32	15	1 .	5	-40 to +85	20	DIP	Pulse output circuit, zero- crossing detector circuit
	TMP4240P,60P,50N, 70N	512 to 1k	32	11 to 23	2.5	5	-40 to +85	16 to 28	DIP,SD	NMOS
	TMP47C200AN/F, 400AN/F,460AN/F	2k to 4k	128 to 256	36 to 58	1.9	5	-30 to +70	42 to 67	SD,Q	LED drivers
	TMP47C210AN/F, 410AN/F,212AN, 412AN	2k to 4k	128 to 256	36	1.9	5	-30 to +70	42 to 44	SD,Q	VFD driver
	TMP47C475AN	4k	256	55	1.9	5	-30 to +70	64	SD	VFD driver, D/A converter with optional PWM output
	TMP47C221AF, 421AF,423AF,425AF	2k to 4k	192 to 256	27 to 28	1.9	5	-30 to +70	64 to 67	Q	LCD driver, OTP option, high speed event counter
	TMP47C231AN	2k	128	24	. 1.9	5	-30 to +70	30	SD	LED drivers, D/A converter with optional PWM output, 4-bit A/D converter
	TMP47C232AN, 432AN	2k to 4k	128 to 256	24 to 36	1.9	5	-30 to +70	42	SD	LED drivers, D/A converter with optional PWM output, 3-state input
	TMP47C233AN, 433AN	2k to 4k	128 to 256	36	1.9	5	-30 to +70	42	SD	LED driver, D/A converter with optional PWM output, 3-bit A/D converter
	TMP47C440AN/F	4k	256	34	1.9	5	-30 to +70	42	SD	LED driver, A/D converter
	TMP47C441AN/F	4k	256	34	1.9	5	-30 to +70	44	Q	VFD driver, A/D converter
	TMP47C446AF	4k	256	24	1.9	5	-30 to +70	64	Q	LCD driver, A/D converter
	TMP47C451AN, 452AN	4k	768	23 to 35	16.7	2.2 to 6	-30 to +70	30 to 42	SD	DTMF generator
	TMP47C456AF	4k	768	35	8.3	2.7 to 6	-30 to +70	80	Q	LCD driver, DTMF generator
	TMP47C25N/F	2k	384	32	8.3	2.5 to 6	-30 to +70	42	SD	DTMF generator
	TMP47C26N/F	2k	384	35	33.3	2.2 to 4.0	-30 to +70	44	Q	DTMF generator
	TMP47C20P/N, 40P/N,46N	2k to 4k	128 to 256	35 to 57	1.9	5	-30 to +70	42 to 64	SD	NMOS, LED driver
	TMP47C800AN/F	8k	512	36	1.3	5	-30 to +70	42 to 44	SD,Q	LED driver
	TMP47C620F,820F	6k to 8k	384 to 512	36	1.3	5	-30 to +70	80	Q	LCD controller/driver, high- speed counter, EEPROM option
	TMP47C434N,634N	4k to 6k	256 to 384	28	1.9	5	-30 to +70	42	SD	Television display on screen circuit, D/A converter with optional PWM output, remot control-circuit LED driver
	TMP47C660,860	6k to 8k	384 to 512	55	1.3	5	-30 to +70	64	SD,Q	A/D converter, remote-control judgment circuit, LED driver OTP and EPROM option
	TMP47C670N,870N	6k to 8k	384 to 512	53	1.3	5	-30 to +70	64	SD	VFD driver, D/A converter with optional PWM output, A/D converter

Key: DTMF = dual-tone multiple-frequency F = flatpack MF = miniflatpack

OPT = one-time-programmable PMP = post-metal programming

Q = quad flatpack
QI = quad in-line flatpack
SD = shrink DIP

VFD = vacuum-fluorescent display

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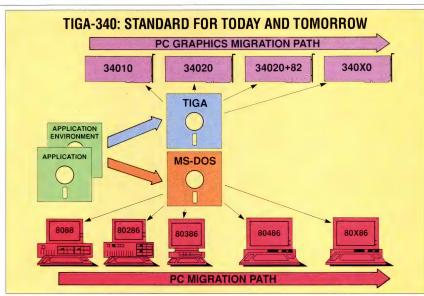
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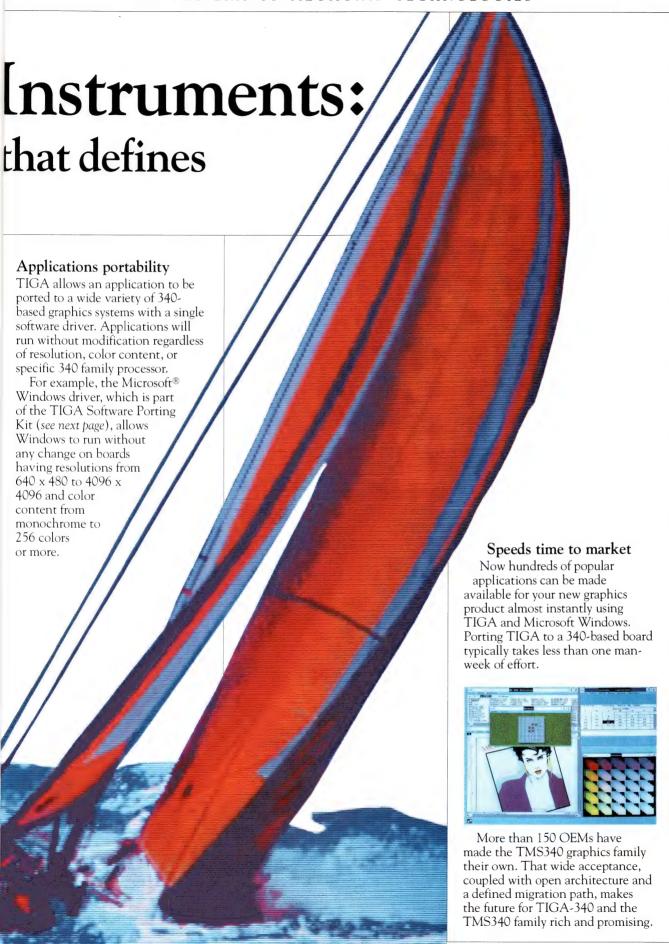


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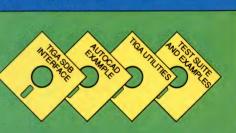
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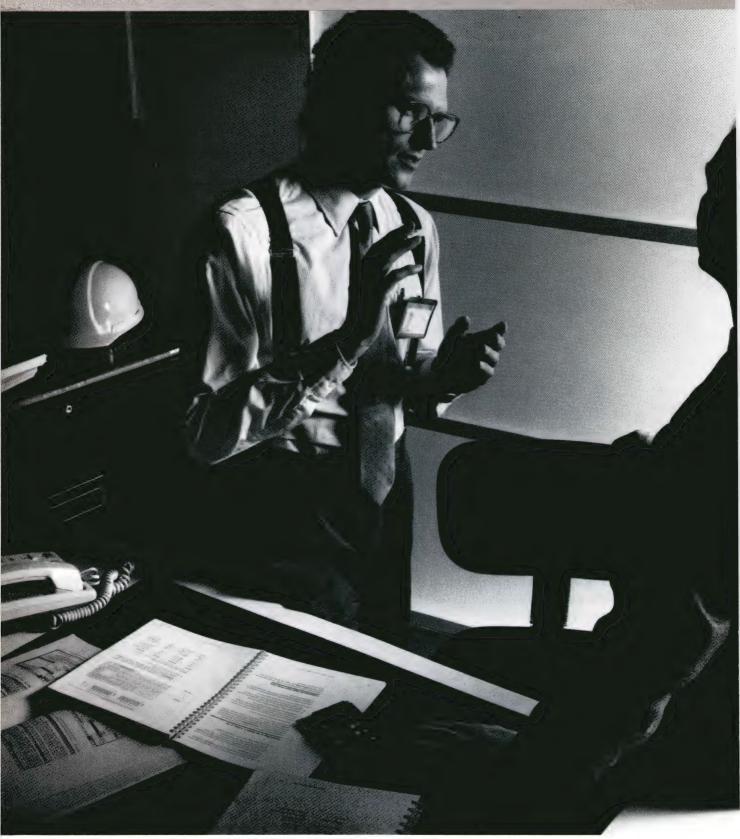


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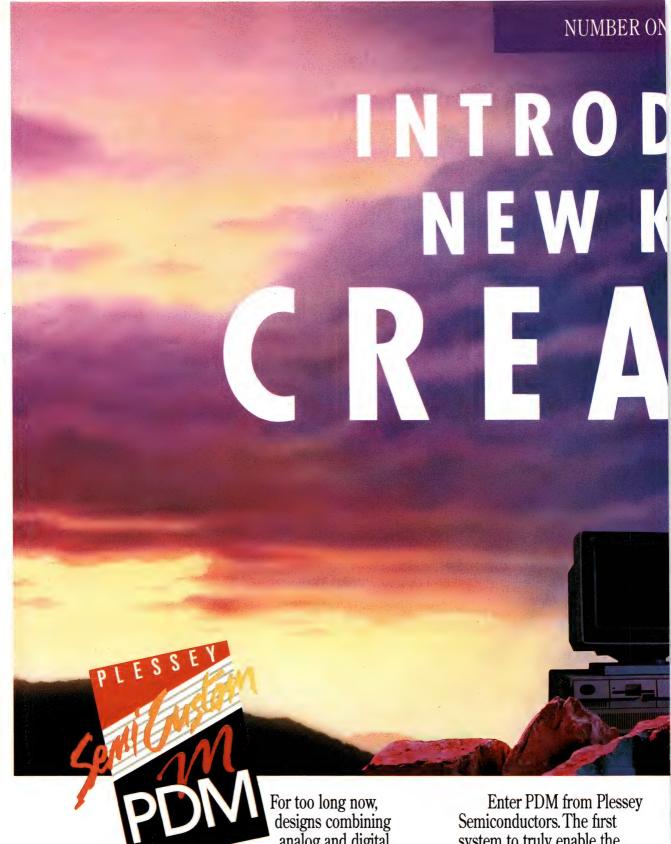
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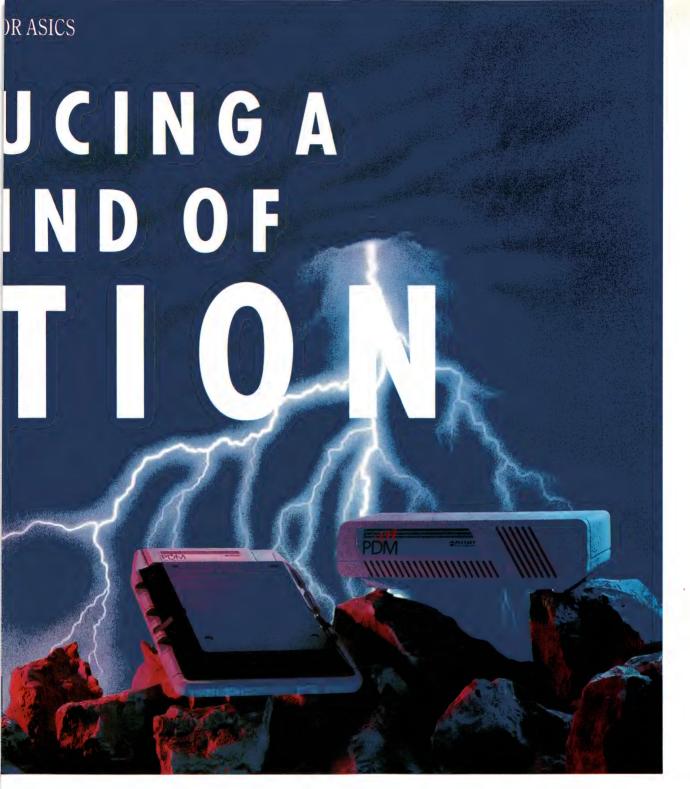


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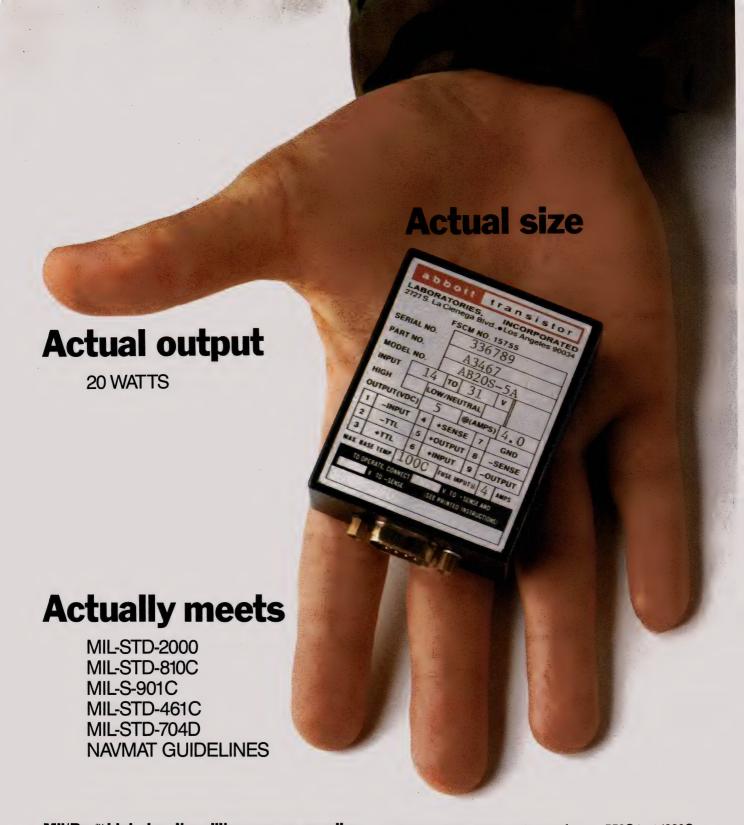


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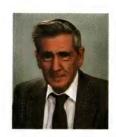
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SEMICUSTOM CIRCUITS

Analog-digital ICs provide versatility



To meet the increasing demand for greater versatility and higher levels of integration, many vendors of semicuston ICs offer chips that contain both analog and digital capabilities.

Dave Pryce,
Associate Editor

ixed-mode semicustom ICs combine analog and digital functions on one chip, freeing system designers from the inherent limitations of early semicustom arrays and the cost penalty of 2-chip sets. Although early mixed-mode chips are still available and often are useful, today's devices generally offer superior performance.

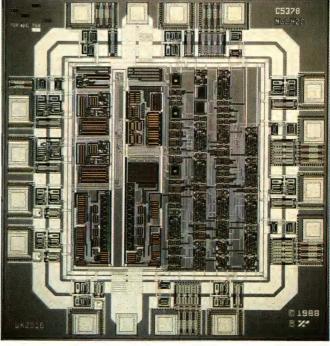
When they first appeared on the market nearly twenty years ago, semicustom ICs were organized into two basic groups—gate arrays and linear arrays—and choosing a suitable device was a relatively simple task. Semicustom chips

still come in these two basic groups, but choosing the right chip requires a lot more awareness today.

For digital circuits, the designer chose a bipolar or CMOS gate array with the appropriate number of gates and the required speed. For analog circuits, the typical choice was a component-based linear array. These arrays, which were usually manufactured in bipolar fabrication, were according to selected the number of transistors, diodes, and resistors needed by the circuit designer.

Most of these firstgeneration linear arrays have a number of intrinsic limitations. For example, because of the component-based layout of these linear arrays, most circuit designs can utilize only about 70% of the available chip area. Another limitation is the disparity in the gain-bandwidth characteristics of the npn and pnp transistors used in these arrays. The dc characteristics of these npn/pnp transistors are also quite different, thus negating the possibility of constructing true complementary circuits.

Apart from their basic limitations, the real problems with most first-generation semicustom chips began when designers wanted both analog and digital functions. At least two chips were needed. Because of differences in processing, op-



Well known for its array-based bipolar chips, Exar also offers semicustom chips based on standard cells. Fabricated using the company's N2000 library, this circuit provides 50% analog and 50% digital functions.

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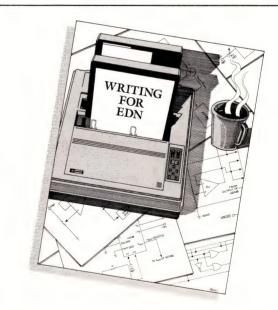
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Semicustom circuits

erating conditions, and dynamic characteristics, the compatibility of the two chips was often less than optimum. Moreover, the additional engineering charge for a 2-chip circuit and the unit cost of a second device were a burden on designers.

Recognizing these problems, vendors began to offer devices containing both analog and digital capabilities. Initially, many of these mixed-mode chips were crude cut-and-paste attempts that provided marginal quantities of gates and linear elements with little, if any, increase in performance.

New-generation mixed-mode chips are superior to their predecessors for a number of reasons. For example, manufacturers have developed more efficient cell-based and scalable architectures that take maximum advantage of the chip's available or allocated real estate. Also, CMOS gates now run at higher speeds while operating at low power.

Linear components improve

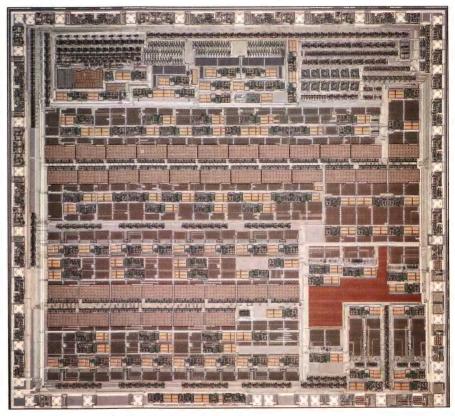
The most noteworthy advances, however, are those made in the linear components. For example, instead of using 5-MHz lateral pnp transistors, many vendors now offer semicustom chips with 200-MHz vertical pnp transistors that match the performance of the vertical npn transistors. This npn/pnp match allows the design of complementary low-frequency and high-frequency circuits. Moreover, many of these chips have redefined the meaning performance; high-frequency some vendors now offer semicustom chips with npn and pnp transistors that have gain-bandwidth products in the gigahertz range.

Adding to the available choices of mixed-mode chips, a number of vendors have mitigated the problems associated with mixed-mode CMOS fabrication and now offer arrays or cell-based chips that offer

both digital and analog functions that provide good performance. Also, many vendors offer chips that have separate low- and high-voltage sections, an architecture that not only extends the chip's voltage rating, but also optimizes its use of real estate. Further, an increasing

fusion mainly arises because of the different kinds of array-based chips.

For example, many of the more recent array-based chips use a tilelike structure, wherein each tile contains a selection of transistors and resistors. Depending on the component content of a particular



This complex circuit was integrated using configurable standard cells. Included on this chip from International Microelectronic Products (IMP) are three DACs, an ADC, a bandgap reference, lowpass filters, a highpass filter, and several other functions.

number of companies offer libraries of standard cells or macro functions that let the user construct a close kin to a full-custom circuit. These libraries often can satisy the requirements of a small system.

If you're going to use a semicustom circuit, you have only two basic choices: array-based or cell-based chips. Cell-based chips may cause confusion because, after fabrication, many of them closely resemble full-custom circuits. A number of subtle differences exist between array-based and cell-based chips, but con-

tile, you use one or more tiles to construct various types of simple analog or digital circuits. To realize the final, complex circuit, you use all or most of the tiles.

Although many array-based chips use a tile- or cell-like architecture, these arrays aren't standard cells. The term *standard cell* refers to complete macro functions such as op amps, comparators, gates, flipflops, and countless other circuit building blocks available in a vendor's library. The term *standard cell* is misunderstood because of its

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original use in compiled, digital CMOS chips, which are essentially machine-crafted, full-custom circuits. Today, standard cells can be semicustom or full-custom circuits. Moreover, standard cells can be analog as well as digital, and they can be manufactured in bipolar or CMOS fabrication, although the latter process is more common.

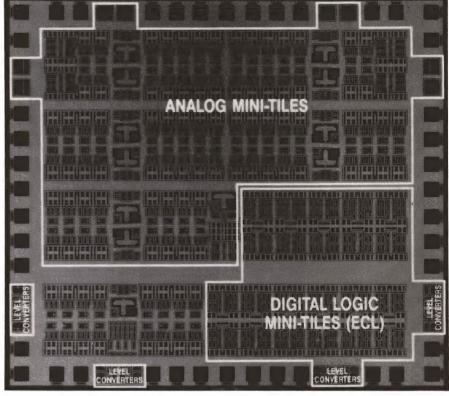
Array-based chips are popular

Whether you choose an array-based or cell-based chip, you're likely to find a mixed-mode semicustom IC that suits your requirements. In recent years, traditional vendors of linear circuits have added new analog-digital arrays to their product lines, and newcomers have jumped into the market with tile-based arrays.

In a departure from its usual component-based arrays, Cherry Semiconductor Corporation (CSC) recently announced its Genesis 97100 servo-driver array. The 97100 is a combination of dedicated macrocells, which are optimized for voice-coil motor applications, and an undedicated area that contains enough components to construct a variety of servo-control functions.

Included on chip is an H-bridge driver, thermal-shutdown circuitry, a current-sensing amplifier, and a dedicated park-head macrocell. You can use the undedicated area to provide specialized control functions such as overcurrent protection and motor braking. The acronym "ASIC" is usually a misnomer, but the 97100 really is application specific.

A relative newcomer, AT&T Microelectronics supplies its ALA501 tile-structured array, which combines 350V-rated DMOS and PMOS linear devices with low-voltage CMOS logic. The mixed-mode array uses dielectric isolation to eliminate the parasitic latch-up problems that often plague junction-isolated tech-



Fabricated in a 1-GHz bipolar process, the FB3631 from Micro Linear is suitable for circuits that require 100-MHz analog bandwidths and 2-nsec ECL gates.

nologies. The ALA501 lets you interface TTL/CMOS logic inputs to high-voltage loads such as a power supply or an ac line.

Included in the ALA501 array are four identical high-voltage tiles, four logic tiles, and a wide variety of uncommitted active and passive components. The high-voltage section contains eight large and eight small DMOS transistors, eight small PMOS transistors, and eight diodes. The logic section features 35 equivalent CMOS gates in a cellular arrangement. Design kits include Spice models, parts for breadboarding, a design guide, and layout plots.

Extending high-frequency performance boundaries is the FB3631 mixed-mode tile array from Micro Linear Corp. Fabricated in a 1-GHz bipolar process, the FB3631 is suitable for designing circuits that require amplifiers with a 100-MHz

bandwidth and ECL gates with delays of 2 nsec. The chip partitions its 144 minitiles into 15 analog-circuit blocks and 66 ECL gates. The total component count includes 690 npn transistors, 154 pnp transistors, and 16 Schottky transistors. Also included is 4778 k Ω of total resistance and 60 pF of MOS capacitance. The FB3631 is typical of new-generation, mixed-mode semicustom chips that use advanced architectures to ease circuit design.

Like Micro Linear, Tektronix uses bipolar processing to extend the high-frequency performance of mixed-mode chips. Its QuickChip-4 modified tile array, for example, combines 6.5-GHz npn transistors with 400-psec ECL gates. For analog design, the QC-4 contains 294 npn transistors, 174 pnp transistors, and 1290 implanted resistors. The pnp transistors are 20-MHz lateral and substrate types. The digi-









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tal section contains 300 equivalent gates. The chip also contains several 1.0- and 2.7-pF capacitors.

Tektronix provides a number of design tools for the QC-4, including a design guide for analog functions, device models for all transistors and resistors in the analog portion of the chip, a design guide for the ECL gate array, logic models for all digital cells, and circuit-simulation software.

Plessey Semiconductors offers a wide range of analog and digital products. The high-performance, bipolar ULA-DF Series is a good example of the company's mixedmode arrays. The DF Series is useful for a wide variety of circuits at frequencies to 100 MHz; the chips feature 1-GHz npn transistors in the analog section and 1-nsec gate delays in the digital section. The total component count for the DF Series ranges from 448 equivalent gates and 32 analog cells for the smallest chip to 2432 gates and 82 analog cells for the largest chip.

Electronic Technology Corp uses a P-well, polysilicon-gate CMOS process to fabricate its AD20Si Series of mixed-mode arrays. Using a 15V supply, the n-channel drivers can provide 20 mA with only a 0.4V drop. The propagation delay for a 2-input NAND gate is typically 3.5 nsec for 5V operation; the delay would be shorter at higher voltages. Laser-trimmed silicon-chromium resistors enhance the performance of analog functions. Available in three sizes, the AD20Si Series provides 4000- and 74CXX-series logic along with analog functions such as op amps, comparators, references, oscillators, and analog switches.

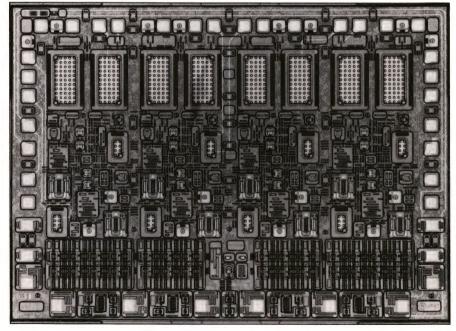
Although array-based semicustom chips remain popular, those based on standard cells are growing at a faster rate. Because of the trend toward mixed-mode chips that combine analog and digital functions, systems designers aren't always able or willing to deal with analog-circuit design at the component level. By using a cell-based chip, designers can use familiar analog building blocks such as op amps, comparators, timers, and references; digital elements such as gates, counters, and flip-flops; and combined functions such as ADCs, DACs, and multiplexers.

Standard cells offer advantages that array-based chips can't provide. For example, because they have no "leftover" components, semicustom chips based on standard cells take maximum advantage of a chip's total real estate. Moreover, it's easier to breadboard a circuit with fully characterized building blocks rather than with individual components. In addition, CAE/CAD tools are generally more effective when used at the macro level.

Exar Corp, one of the pioneers of linear semicustom arrays and the company that recently introduced its novel Flexar-Delta arrays, also offers standard-cell chips. The company's N2000 library of analog and digital standard cells, which is fabricated in a 2-µm BiCMOS process, provides fast digital switching, precise analog functions, and dense memory, including EEPROM.

The N2000 library includes 125 digital cells, 50 analog cells, and 25 memory macros of EEPROM, RAM, and software-configurable ROM. The digital cells feature toggle frequencies to 75 MHz and a typical propagation delay of 1 nsec for a 2-input NAND gate. The analog cells include op amps, comparators, oscillators, switched-capacitor filters, ADCs, and DACs.

SGS-Thomson Microelectronics features several types of semicustom chips, including the tile-based, bipolar TSFJ Series and the cell-based, CMOS TSGSM Series. The TSGSM chips are suitable for designing high-performance analog and digital circuits. The TSGSM library includes 94 logic cells and 66 analog cells. Also included are TTL-



This tile-structured array, the ALA 501 from AT&T Microelectronics, features 350V-rated DMOS and PMOS linear devices with low-voltage CMOS logic. The mixed-mode chip uses dielectric isolation to eliminate the latch-up problems that often occur in junction-isolated devices.

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and CMOS-compatible I/O cells.

The TSGSM chips' digital functions can achieve operating speeds to 15 MHz. Bandwidths for representative analog functions range from 3.3 MHz for a general-purpose op amp to 10.5 MHz for a transconductance amplifier. The analog-cell library also includes a 12-MHz crystal oscillator, 8- and 12-bit A/D converters with 25-µsec conversion times, a 1.2V bandgap reference, and a comparator.

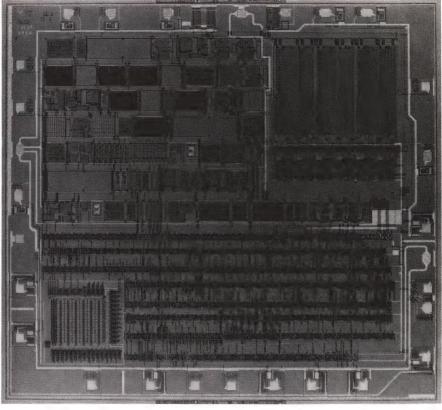
CAD tools include schematic capture, logic and analog simulations, automatic place-and-route capability, and test-pattern generation. These tools are available on DEC's VAX computer systems. In addition, the TSGSM library is implemented on Daisy, Mentor, and SUN CAE workstations.

National Semiconductor's semicustom product line is called CLASIC (Customizable Linear Application Specific Integrated Circuits). The CLASIC library of analog and digital standard cells includes a choice of bipolar (LFAST) or CMOS (LCMOS) technologies.

The LFAST bipolar process features npn transistors that have an f, of 2.5 GHz; the gain-bandwidth product of the pnp transistors is in the 40-MHz range. The high-density capability of LFAST lets you build circuits that contain more than 100 equivalent op-amp functions, along with digital logic circuitry. The op amps have bandwidths to 25 MHz, and logic functions have typical gate delays of 1.5 nsec and toggle frequencies of 140 MHz.

LCMOS, a 3- μ m CMOS process, is tailored for combined analog-digital applications. Op-amp functions have bandwidths of 5 MHz and offset voltages of <5 mV. Logic functions have gate delays of 5 nsec and toggle frequencies of 20 MHz.

The CLASIC standard-cell library contains over 400 cells, in-



Using standard cells, this circuit provides several functions. Implemented with the CMOS TSGSM library from SGS-Thomson Microelectronics, the chip contains several op amps, a sixth-order switched-capacitor filter, an 8-bit A/D converter, several capacitors, and a section of digital gates.

cluding op amps, comparators, logic blocks, data-acquisition circuits, voltage references, and peripheral cells. The library also features individual npn and pnp transistors and a selection of resistors and capacitors. Using the library's PC-based design tools, you can perform schematic capture and simulation of the cells in the library.

Sierra Semiconductor claims to have the largest library of standard cells available. A review of the company's catalog makes this claim believable. The SCDS (Sierra Custom Design System) library includes nearly 400 cells in 2-µm CMOS technology and 300 cells in 1.5-µm CMOS technology. The variety of cell types is also extensive. Among other functions, the library includes ADCs, DACs, buffers, op amps, multiplexers, microcontroller cores,

flip-flops and latches, arithmetic functions, oscillators, PLLs, comparators, and 32- to 4k-bit EEPROMs.

The performance of the SCDS standard cells is also noteworthy. The library's digital cells operate as fast as 70 MHz and feature 120-MHz toggle rates, and the analog cells operate as fast as 65 MHz. The company also offers 10-MHz resistor DACs, 100-MHz video DACs, and fast (10 nsec) comparators.

Vital to Sierra's library of standard cells is its Montage software system, which is structured on Silicon Compiler Systems' (San Jose, CA) software modules. According to Sierra, this software permits a system engineer to design, develop, and simulate complex mixed-mode circuits at his own desk using integrated CAE-design tools and Unix-



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based workstations, such as those from Sun Microsystems (Mountain View, CA) and the Apollo Computer Div of Hewlett-Packard (Palo Alto, CA).

Configurable standard cells

Unlike many manufacturers, International Microelectronic Products (IMP) offers a library of configurable CMOS standard cells for its mixed-mode semicustom chips. IMP, like Gould/AMI, uses its analog standard cells only as a starting point. From that point, it modifies the cells according to specific customer needs. This configurability enables IMP to limit the total number of analog cells in its library and

still satisfy most requirements. IMP uses an in-house automated-design system to perform the tasks of schematic capture, simulation, physical layout, and test.

Gould AMI has several libraries of standard cells, including its CCI family. Fabricated using a 3-µm CMOS process, the CCI cells are intended primarily for combined analog-digital applications; the analog portion of the cell operates at 10V, and the digital portion operates at 5V. Gould also offers its ABX family of cells, which includes electrically erasable ROMs, implant-programmable ROMs, and bipolar transistors.

NCR has three libraries of analog

standard cells, as well as libraries of digital functions, compiled functions, and supercells. The analog li-1.7-µm braries comprise the VS2000 Series, the 1.1-µm VS1500 Series, and the 0.7-µm VS700 Series. These libraries contain numerous analog cells including op amps, comparators, references, VCOs, ADCs, and DACs. The digital libraries include a variety of gates. flip-flops, shift registers, counters, RAMs, ROMs, EEPROMs, multiplexers, and µCs.

Standard Microsystems' library of 1.6-, 2.0-, and 3.0-µm CMOS standard cells has far more digital functions than analog functions. The library contains nearly 200

For more information . . .

For more information on the semicustom products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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cells, including a complete library of 74LS SSI and MSI logic functions. Also included are a number of analog cells such as op amps, comparators, references, and several supercells for RAM, ROM, UART, μP , and VCO functions.

Standard cells attain 2 GHz

Although the array-based bipolar QC-4 chip from Tektronix is sufficiently fast, it can't match the blazing speed of the standard cells from its subsidiary company, TriQuint Semiconductor. Using an advanced GaAs technology, TriQuint achieves 2-GHz performance with its line of digital standard cells and analog macro functions.

The typical delay for a 2-input NOR gate is only 95 psec, and a flip-flop's typical delay is 170 psec. TriQuint maintains that its GaAs technology has a better speed/ power product than does bipolar ECL. The analog macro functions include an op amp with a 1-GHz bandwidth, a buffer amp with a 2-GHz bandwidth, laser drivers with rise and fall times of 100 psec, transimpedance amplifiers, and 4- and 8-bit DACs. The company offers standard-cell libraries for Daisy and Mentor workstations and a manual with circuit-design guidelines.

A different choice

Advanced Linear Devices (ALD) takes a different approach to the construction of semicustom circuits. Instead of providing array- or cell-based chips, the company takes its building blocks from its own function-specific line of standard products. These fully characterized building blocks include linear functions such as op amps, comparators, timers, and matched n-channel and p-channel dual MOSFETs. Digital functions are replicated from any 74HC- or 4000-series logic devices.

ALD offers a library of 38 of these standard products—or "standard cells"—including gates, flip-flops, shift registers, and counters.

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This review provides only a limited sampling of the available mixed-mode semicustom chips. The number of semicustom circuits will continue to increase rapidly, with the emphasis on combined analog-digital capability. Although today's semicustom chips are far superior to those of a few years ago, the choices aren't as simple anymore. Before choosing a chip, you must carefully consider a wide range of performance capabilities, architectures, and process technologies.

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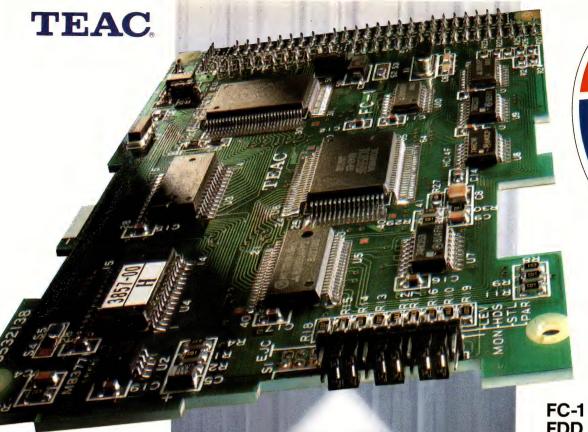
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	TCR	±250 PPM /°C	±100 PPM/°C	_
	TRACKING TCR	±100 PPM/°C	±10 PPM/°C	-
=	LOAD WATTAGE	150mW/MM ²	_	_
RESISTUR	RESISTOR TOLERANCE	> ±1.0%	+0.3%	. –
RES	STABILITY: TEMPERATURE HUMIDITY HEAT CYCLE	± ±1.5% ± ±2.0% ± ±2.0%	-	430°C, 5 MIN. 60°C, 95% 125°C↔-40°C
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U169SCPB-L	1 × 16	9.0	Р	. х	
U205SCPB-S	1 × 20	5.0	S/P		
U209SCPB-L	1 × 20	9.2	Ρ.	х	
U2015SCPB-L	1 × 20	15.1	Р	х	
U406SCPB-S	1 × 40	5.0	Р	Х	
U20026SCPB-S	2 × 20	5.1	Р	х	х
U40026SCPB-S	2 × 40	5.0	Р	х	Х
CU40046MCPB-S	4 × 40	5.0	S/P	х	х
CU40066MCPB-S	6 × 40	5.0	S/P	х	х
CU40086MCPB-S	8 × 40	5.0	Р	х	х
	J209SCPB-L J2015SCPB-L J406SCPB-S J20026SCPB-S J40026SCPB-S J40046MCPB-S J40066MCPB-S	1 × 20 12015SCPB-L	1 × 20 9.2	1 × 20 9.2 P	1 × 20 9.2 P x 209SCPB-L 1 × 20 9.2 P x 201SSCPB-L 1 × 20 15.1 P x 400SCPB-S 1 × 40 5.0 P x 20026SCPB-S 2 × 20 5.1 P x 40026SCPB-S 2 × 40 5.0 P x 40026SCPB-S 4 × 40 5.0 S/P x 40066MCPB-S 6 × 40 5.0 S/P x

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DOT MATRIX FORMAT (DOTS/LINE × NO. OF LINES)	MODEL NUMBER	NO. OF LINES AND CHARACTERS/LINE (5x7 DOT CONFIGURATION)	GRAPHICS CAPABILITY
192 × 16 (3072 DOTS TOTAL)	GU192X16	2 × 32	YES
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256 × 64 (16,384 DOTS TOTAL)	GU256X64	8 × 42	YES

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Analog comparators mate with ECL, TTL



Designers in both the ECL and TTL camps are reaping the benefits of a new generation of fast, high-precision linear comparators.

Bill Travis,Contributing Editor

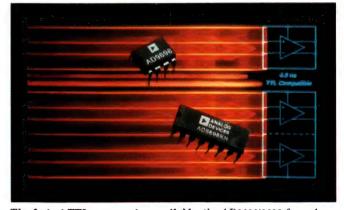
either TTL nor ECL is a clear-cut winner in the battle for supremacy in IC design. ECL still maintains its edge in speed, though lower-power TTL circuitry is making steady advances in this crucial parameter. Manufacturers of analog comparators are covering their bets by developing new products that satisfy both the TTL and ECL camps. Advances in semiconductor-processing techniques have endowed a number of recent devices with increased speed and precision.

Table 1 provides the vital specifications of recently announced ECL-compatible linear comparators, and Table 2 presents the salient features of recent TTL-compatible linear comparators. Like so many ICs, these devices merit the adjectival phrase "application specific." For example, consider the very fast, ECL-compatible parts in Table 1. Suppose your application entails 12-bit A/D conversion. A glance at the "OD" (overdrive) qualifier in Table 1 reveals

that the only suitable new device is Harris's HF-0003, slated for release in the second quarter of this year. One LSB in a 12-bit, 10V system is about 2.4 mV; the Harris device is the only one that has enough gain to allow a propagation-delay spec with 1-mV overdrive. Note that in almost every comparator data sheet, the overdrive is specified with a 100mV step. Therefore, in the case of the Harris device, whose inputs are set for a switching threshold of 100 mV, the input pulse to yield a 4.3-nsec-max propagation delay would be 101-mV high.

Another important consideration in your choice of comparators is the cleanliness of the output switching waveform. If a comparator doesn't have built-in hysteresis (different switch-high and switch-low thresholds), its output will chatter as the input voltage slowly passes through the threshold.

The data sheets for Maxim's ECL-compatible parts are unequivocal on the point of output chatter. The data sheet for the MAX9685, for instance, states that, to avoid output chatter, the minimum input-signal slew rate should be 1.6V/µsec, equating to minimum signal amplitudes of 360 and 90 mV rms at frequencies of 500 kHz and 4 MHz, respectively. If the minimum expected signal amplitudes in your application allow you to apply hysteresis, you can avoid or reduce the chatter by adding hysteresis at the input. Fig 1a shows

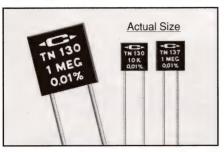


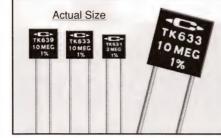
The fastest TTL comparator available, the AD9696/9698 from Analog Devices, features a 7-nsec propagation delay. Its data sheet includes a useful parameter called dispersion—the variation in propagation delay as a function of input overdrive.

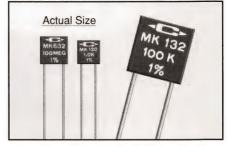
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0.50 Watt (CK05), 0.75 Watt (CK06)

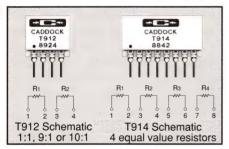
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- Space Efficient Radial-Lead Design

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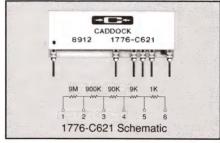
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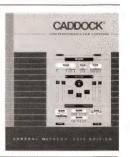
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TECHNOLOGY UPDATE

Analog comparators

you how to add dc hysteresis; in **Fig 1b**, the use of ac regenerative feedback reduces the minimum allowable input slew rate by a factor of four.

LeCroy's MVL407 quad comparator eliminates chatter by using built-in 4.8-mV hysteresis. The high-switching input threshold is typically +2.4 mV, and the low-switching point is typically -2.4 mV. The 4.8-mV hysteresis, of course, disqualifies the device for A/D applications in which the resolution is greater than 10 bits.

Model HVL407 meets the needs of ATE (automatic test equipment) applications by providing an input range of -2.5 to +10.5V. This device, basically an enhanced, hybrid version of the monolithic MVL407, has FET inputs to reduce the 407's input-bias current from 5 μ A to 40 nA. The 407 also provides hysteresis at the input to eliminate output chatter. It's available in two versions: four independent channels or

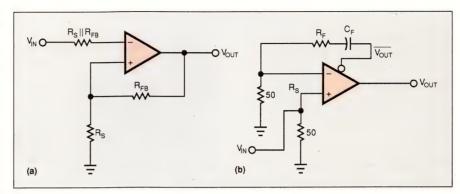


Fig 1—Adding hysteresis eliminates transitional chatter in a comparator's output characteristic. The configurations in **a** and **b** use positive (regenerative) feedback—dc and ac coupled, respectively—to add snap action to the comparator's switching characteristic.

two window-configured comparator channels.

LeCroy's Model HVL100 discriminator takes the MVL407 one step further. The hybrid combines the 407 with a Motorola 10198 monostable multivibrator to form a single-channel comparator that generates a pulse. You set the width of the pulse by using an appropriate external resistor and capacitor. Three sections of the internal

MVL407 form a threshold detector, a pulse stretcher, and a driver for the multivibrator; the fourth section serves as the discriminator's output driver.

A wide -3-to-+10V input range makes the HCMP96900 dual comparator from Signal Processing Technologies (formerly Honeywell SPT) suitable for ATE applications. Its predecessor, the HCMP96870, had an input range of only -2.5 to

Table 1	-Recen	ECL.	comp	atible	linear	compa	rators
	,	,		1		,	

Manufacturer	Model	Туре	Single/ dual/ quad	Propagation delay (nsec)	current	Offset voltage (mV max)	Input range	Price	Comments
Harris	HF-0003	Mono- lithic	Single	3.4 max (5-mV OD) 4.3 max (1-mV OD)	12	5	-2.9 to +4.8V (+5, -5.2V supplies)	To be determined	Introduction slated for second quarter of 1990.
Lecroy	MVL407	Mono- lithic	Quad	4 max (50-mV OD)	7	Not available	-2 to +1.7V (+5, -5.2V supplies)	\$13.50	Typical dispersion 100 psec for 5- to 100-mV inputs.
	HVL407	Hybrid	Quad	6 max (800 mV p-p)	0.04	10	-2.5 to +10.5V (+20, -5.2V supplies)	\$160	Enhanced hybrid version of MVL407 monolithic comparator.
	HVL100	Hybrid	Single	16±2	3.5	4	-2 to +2V (+5, -5.2V supplies)	\$97	Combines MVL407 with 10198 monostable to form discriminator.
Maxim	MAX9690	Mono- lithic	Single	1.8 max (10-mV OD)	20	5	-2.5 to +2.5V (+5, -5.2V supplies)	\$3.70 (100)	Available in DIP, ceramic DIP, and SO package.
	MAX9685	Mono- lithic	Single	1.8 max (10-mV OD)	20	5	-2.5 to +2.5V (+5, -5.2V supplies)	\$3.80 (100)	Latchable version of MAX9680.
	MAX9687	Mono- lithic	Dual	1.9 max (10-mV OD)	20	5	-2.5 to +2.5V (+5, -5.2V supplies)	\$6.33 (100)	Dual version of latched MAX9685.
Signal Processing Technologies	HCM96900	Mono- lithic	Dual	5 typ (100-mV OD)	20	3	-3 to +10V (+12, -7V supplies)	\$16 (100)	Inputs protected to 1V beyond supplies. Responds to < 1.5-nsec-wide glitches.

Notes

EDN March 1, 1990

OD-overdrive; IE-the amount by which the input step surpasses the triggering threshold.

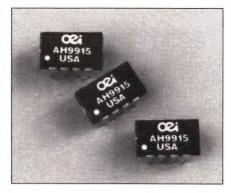
TECHNOLOGY UPDATE

Analog comparators

+2.5V. An added bonus with the HCMP96900 is the input protection it provides against signals that exceed the supply rails (by as much as 1V). This feature allows you to connect simple, inexpensive diode clamps to the supplies to limit the inputs.

TTL creeps up on ECL

Because it uses a single 5V supply and has lower power dissipation, TTL is the logic system of choice for many designers. Semiconductor-processing advances such as full-complementary structures and dielectric-isolation fabrication that can be done at a reasonable cost-are shrinking the onceimmense speed edge ECL had over the TTL system.



This single-supply comparator accepts input levels equal to the full power-supply span. The AH9915 from Optical Electronics drives six standard TTL loads.

Two recent comparator families from Analog Devices and Maxim Integrated Products (Table 2) are good examples of just how fast TTL can get. Analog Devices' AD9696/

Table 2—Recent TTL-compatible linear comparators

9698 single/dual device has a propagation delay of only 7 nsec max with 20-mV overdrive. The units operate from either one 5V supply or dual ±5V supplies. Useful in timing circuits in ATE or communications applications, the 9696/9698 provides a latch-enable input; the setup time for the latch is 1.7 nsec. One useful specification the company provides propagation-delay dispersion, which consists of the delay changes by 200 psec max for input overdrives from 50 mV to 1V.

The single/dual MAX9686/9698 from Maxim features a 9-nsec-max propagation delay with 10-mV overdrive. Pin compatible with industry-standard LT1016 and Am686 units, the 9686/9698 works from +5and -5.2V supplies. Like the Ana-

standard TTL loads

Manufacturer	Model	Single/ dual/ quad	Propagation delay (nsec)	current	Offset voltage (mV max)	Input range	Price (100)	Comments
Advanced Linear Devices	ALD4302	Quad	400 typ (5-mV OD) 120 typ (TTL step)	220 pA	5	-0.3 to +3.5V (5V supply)	\$2.28	Improved version of industry-standard LM339. Outputs can sink or source current. Outputs usable in wired-OR or push-pull mode.
Analog Devices	AD790	Single	40 typ (5-mV OD)	3.5 μA	0.25	-Vs to +Vs -2V	\$2.50	Built-in 0.5-mV hysteresis. Works from 5 or 15V supplies. Output is TTL and CMOS compatible.
ř	AD9696/ 9698	Single/ dual	7 max (20-mV OD)	35 μΑ	2	-2.2 to +3.7V (±5V supplies) 1.4 to 3.7V (5V supply)	\$3.50/\$6.00	Accommodates TTL or CMOS supplies. Available in DIP, ceramic DIP, metal can, and SO package.
Elantec	EL2252	Dual	7 typ (200-mV OD)	12 μΑ	6	-9 to +10V (±15V supplies)	\$5.03	Outputs adaptable to TTL or CMOS levels. Intended as pin receiver in ATE systems.
Linear Technology Corp	LT1015	Dual	14 max (20-mV OD)	30 μΑ	201	1.5 to 3.5V (5V supply)	\$4.20	Intended as line receiver for backplanes. Output stage eliminates supply glitching.
Maxim	MAX9686/ 9698	Single/ dual	9 max (10-mV OD)	25 μΑ	3	-3 to +3V (±5V supplies)	\$3/\$4.80	Pin-compatible with LT1016 and Am686. Has latch with 2-nsec setup time.
National Semiconductor	LM613	Dual	1500 typ (TTL swing)	20 nA	2.5	-VS to +VS-1.4V	\$1.30	Package contains two op amps, two comparators, and adjustable 3-terminal regulator.
Optical	AH9915	Dual	55 max	20 μΑ	70	0 to 5V	\$23.75	Outputs sink and source currents. Drives six

(5V supply)

Notes:

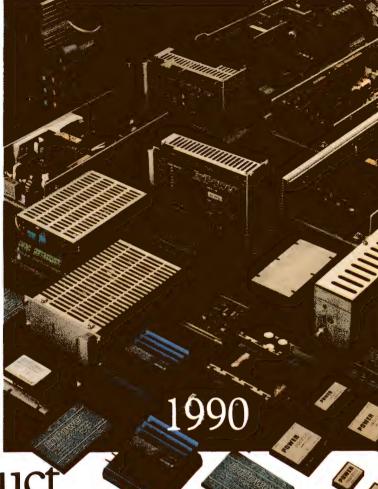
Electronics

- 1. Maximum required to drive output to 0.5V low state and 2.5V high state
- 2. OD-overdrive; IE-the amount by which the input step surpasses the triggering threshold

(30-mV OD)

35 max (100-mV OD) 15 max (1V OD)





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which can be used to realize distributed power architecture.

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TECHNOLOGY UPDATE

Analog comparators

log Devices units, the 9686/9698 comparators provide a latch-enable input. The setup time is 2 nsec typ.

An improved version of the industry- standard LM339 quad comparator, the ALD4302 from Advanced Linear Devices, uses silicongate CMOS processing to keep power dissipation to just 150 μ W per section. It improves upon the LM339 in speed (120- vs 300-nsec propagation delay) and output structure—it can sink and source

currents (the LM339 has open-collector outputs). Further, the 4302's input impedance is much higher; its input-bias current is 200 pA max vs the LM339's 250 nA max. Advanced Linear Devices also offers the 4302 as a standard cell in its ASIC portfolio.

Elantec's speedy EL2252 dual comparator, which is intended as a pin receiver in ATE and data-communications applications, is also application specific. Its wide -9 to

+10V input range makes it suitable for ATE systems. To facilitate the elimination of output chatter, the 2252 provides a hysteresis pin. Tying this terminal to the negative rail produces approximately 60 mV of hysteresis in the input function. Another nice touch is a TTL pin: When grounded, it yields TTL outputs; when open, it produces CMOS outputs.

Another application-specific comparator is Linear Technology's

Follow guidelines when using monolithic comparators

Comparators may be the most underrated and underutilized of linear monolithic components. This second-class citizenship is unfortunate, because the comparator is one of the most flexible and universally applicable components. These devices sometimes suffer from erratic operating modes and oscillation, but usually you can trace these problems to one or more specific areas.

Brute-force "solutions" to problems such as oscillation can mask or actually cause errors. In troubleshooters' frantic attempts to eliminate oscillation, many bypass capacitors have been wasted. Therefore, simply stopping the oscillation doesn't guarantee a satisfactory solution. To provide a genuine cure, especially in the case of oscillation, it's crucial that you confront the real cause of the problem and test the theory behind your remedy, even if your remedy seems to work.

Board layout and power-supply connections require close attention. Fast comparators necessitate a ground plane and always require supply bypassing. To minimize stray capacitance, input connections should always have small trace areas. You can reduce the strays by placing input-connected components near the comparator. In addition, you should drive comparator inputs with the lowest practical source impedance to reduce the effects of residual stray capacitances. This low source impedance is particularly important with fast devices. To prevent parasitic coupling, route outputs away from inputs and offset pins. In addition, evaluate comparator load currents, both transient and dc, to avoid unwanted feedback through the ground and powersupply lines.

All comparators have input common-mode restric-

tions to which you must adhere. Maintain the input levels within specified limits at all times. It's easy to predict dc conditions, but ac phenomena are more subtle. Carefully evaluate the undesirable effects that input and feedback capacitors can produce. Often, a capacitor's differentiated response can cause input excursions that exceed the stipulated limits.

It's wise to consider the effects of the variation of the common-mode rejection ratio vs input signal level. For precision work (0.1% accuracy or better), single-ended crossing detectors (one input held at a dc level) are usually preferable to circuit configurations in which you can apply ac signals to both inputs.

Device gain and offset are additional issues you must consider, particularly for fast comparators. In general, the faster the device, the lower the gain. Gains range from 1000 to 1,000,000 V/V or more for slow comparators. Be sure the comparator has enough gain to fully switch for the lowest anticipated input overdrive. Also, remember to include the effects of input offset error.

Finally, always take probe-induced errors into account. A poor probing technique can cause apparent errors or oscillation. When you're evaluating the circuit, keep dc and ac loading effects in mind. At high speeds, probe ground straps are often parasitic sources that introduce bizarre effects. Use probe-tip grounding attachments with direct ground-plane connections at the point of measurement. When you've finished, put these attachments in your desk and don't loan them to anyone. I, for one, won't even admit I own them.—Jim Williams, Contributing Editor



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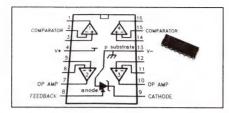
TECHNOLOGY UPDATE

Analog comparators

LT1015, which is intended as a line receiver in backplanes. This part is designed not to chatter or oscillate when the output switches. No minimum slew rate is required on the inputs. The company also claims that the output structure virtually eliminates power-supply glitching during transitions—a traditional gremlin in TTL comparators. An on-chip latch-enable function has a setup time of 2 nsec typ.

Another chatterless unit is Analog Devices' AD790, which features 0.5-mV built-in hysteresis. The company maintains that the 790's output structure eliminates the traditional pnp-npn current spikes during transitions. Other features include a latch-enable pin, the ability to source or sink 10 mA, and a separate logic-supply pin for the output stage. The 790 has the lowest offset voltage (0.25 mV max) of all the units reviewed here.

The LM613 from National Semiconductor contains an abundance of circuit functions. The package has two op amps, two comparators, and an adjustable 3-terminal regulator. A member of the family the com-



A jack-of-all-trades building block for analog systems, the LM613 from National Semiconductor includes two op amps, two comparators, and an adjustable 3-terminal regulator.

pany calls "Super-Block" circuits, the 613 draws an operating current of 1 mA max. Its op amps resemble LM324 types, and the comparators are similar to the industry-standard LM339. The 613 can operate with power-supply spans from 4 to 36V.

A speedy unit (15-nsec max with 1V overdrive) from Optical Electronics operates from one 5V supply and accepts input voltages from ground to the supply level. The AH9915 requires a minimum input overdrive of 30 mV; its output structure sinks and sources enough current to drive six standard TTL loads.

Finally, not included in **Table 1** or in **Table 2**, the MB4205 from

Fujitsu Microelectronics is a bruteforce, lamp-driver comparator that sinks currents as high as 0.5A. Intended principally for automotiveelectronics applications, the 4205 includes an on-chip constant-current source that you can use to make resistance comparisons at the inputs. It accepts input voltages from ground to 2V less than the positive supply. The comparator costs \$0.95 (1000).

The sole Japanese-owned company to respond to editorial calls for this report—Fujitsu—is evidently serious about marketing its linear products in the US. The company offers several industry-standard comparators, including pinfor-pin equivalents to the LM393, LM339, and CD4002.

Reference

"High-Speed Comparator Techniques," Linear Technology Corp Application Note 13.

Article Interest Quotient (Circle One) High 509 Medium 510 Low 511

For more information . . .

For more information on the analog comparators discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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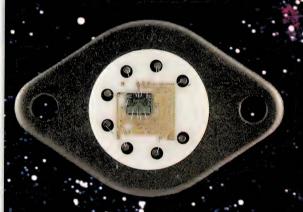
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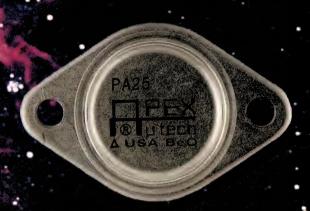


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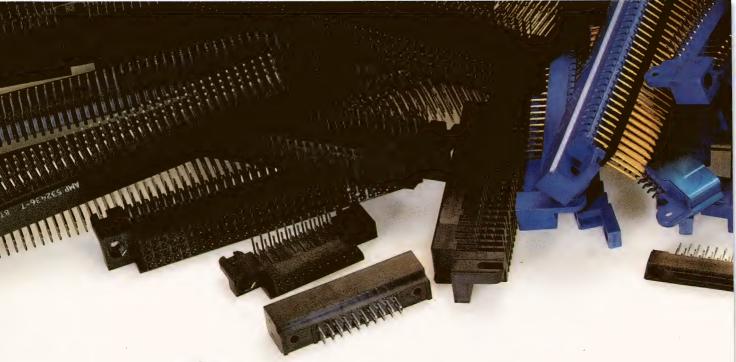


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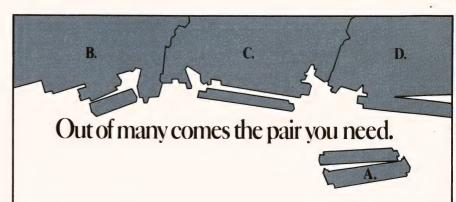
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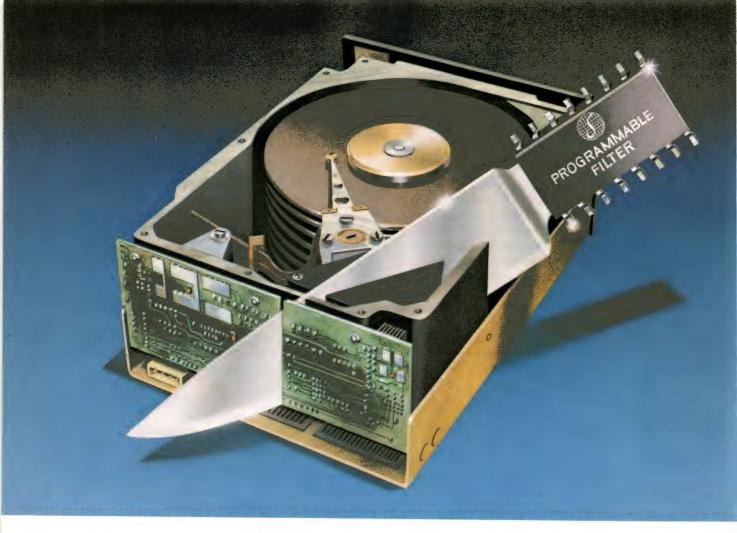
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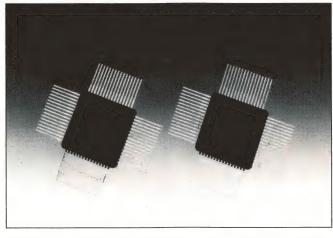
lthough the dynamic RAM (DRAM) is the cornerstone of a personal computer's memory, it is the static RAM (SRAM) that's enabling designers to produce the new generation of high-performance workstations and supercomputers. Unlike DRAMs, which need periodic refreshing, SRAMs are always ready to respond to system needs.

Also driving the demand for faster SRAMs is the increasing use of ECL technology for

CPUs that operate between 80 and 200 MHz. For these applications, manufacturers often use self-timed synchronous SRAMs, which are substantially faster than conventional asynchronous SRAMs.

To meet the need for faster SRAMs, National Semiconductor has fabricated the NM4492 and NM100492 series of $2k \times 9$ -bit Advanced Self-Timed (AST) SRAMs. Implementing the company's advanced BiCMOS-III process, the AST SRAMs combine the low power and high density of CMOS with the high speed of ECL-compatible bipolar circuitry.

Unlike conventional SRAMs, self-timed SRAMs contain on-chip functions that speed up operation and simplify critical write-cycle timing. First, inputs and outputs are registered or latched, and their timing is controlled by a clock input that synchronizes the SRAM operation with the system timing. Sec-



Packaged in 64-lead quad flatpacks, these Advanced Self-Timed (AST) static RAMs feature synchronous operation. Available in access-time ratings of 5-, 7-, and 10-nsec, these memory chips can work with CPUs operating in the 80- to 200-MHz range.

ond, the chip self-times the complicated write cycle by means of an on-chip write-pulse generator. These functions not only relieve system designers of some difficult timing problems, but also simplify the external circuit requirements.

Compared with other self-timed SRAMs, AST SRAMs include additional on-chip features such as a timing generator for the output registers, parity checking of both data and address inputs, and clock gating that simplifies the control of pipelined operations. Furthermore, AST SRAMs feature maximum access times of 5 to 10 nsec, enabling system designers to improve high-speed CPU performance by 60 to 150% over standard SRAMs and other self-timed SRAMs.

For example, the NM4492W5, which has an access time of 5 nsec, allows 5-nsec system cycle times as well. Comparable products such as a 13-nsec self-timed synchronous

SRAM achieve cycle times of 15 nsec in the system; a 10-nsec asynchronous SRAM will achieve cycle times of 15 to 20 nsec in the system.

AST SRAMs also provide decision-making logic for output register timing, which can implement a "hidden" write-cycle mode. In this mode, AST SRAMs can write while the system is reading the output register, thus interleaving reads and writes and improving system performance. Another feature provides

on-chip scan diagnostics, which allows automated self-checking of SRAM operation.

All five of the company's AST SRAMs have F100K I/O levels and come in 64-lead ceramic quad flatpacks. Depending on operating speed, power requirements range from 1.6 to 2.7W. The 5-nsec NM4492W5, 7-nsec NM4492W7, and 10-nsec NM4492W10 devices operate from a -5.2V supply; the 7-nsec NM100492W7 and 10-nsec NM100492W10 devices operate from a -4.5V supply. Unit pricing in 1000-piece quantities is \$149 for 5-nsec versions, \$106 for 7-nsec versions, and \$96 for 10-nsec versions. Production is scheduled for the third quarter.—Dave Pryce

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Daisy, Mentor, and Valid work-stations support these sea-of-gates arrays, which have base configurations offering 10,000 to 100,000 usable gates (at 40% utilization) and 144 to 408 I/O pads. In addition, third-party software support from Synopsis' logic synthesis tool and Cadence's Verilog XL simulator is available.

The HG62S arrays use library cells compatible with the vendor's earlier array families. The library of more than 300 macros includes as much as 64k bits of 12-nsec static RAM. Scan macros, which you can use with automatic test-pattern generation (ATPG) software, facilitate testing. Peripheral cells in-

clude I/O buffers with slew-rate control and high-drive current buffers, which can deliver 48 mA.

The vendor built the arrays using a 0.8-µm (drawn), 3-layer metal process. The cost, as with any ASIC, depends on the complexity and volume of your design and the level of support you require from the vendor. The suggested piece price will generally vary from \$10 to \$300, and NRE costs will typically range from \$20,000 to \$140,000.—Michael C Markowitz

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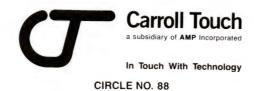


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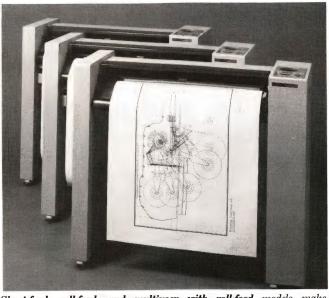
Plotter family uses HP-GL/2 language and has pen and electrostatic offerings

The Draftmaster family of pen plotters and the HP 7600 family of electrostatic plotters provide support for the HP-GL/2 graphics language. This language uses polyline encoding, which reduces the amount of data a host must transmit to a plotter. An E-size color unit in the electrostatic family costs \$45,900, including a 1-year warranty. The pen-plotter family features multiuser capabilfaster drawing ity, speed, and a pen that's disposable.

The Draftmaster family provides three types of feeders: the sheet-feed

SX model; the roll-feed RX model; and the multiuser MX model, which also has a roll feeder. The units cost \$8495, \$9995, and \$11,995, respectively, and provide a 1M-byte buffer. The MX model contains four I/O ports to accommodate four users and a 20M-byte disk drive to queue incoming plots. An operator can monitor the queue from the plotter front panel and set priorities for plots in the queue. The front-panel controls of all three units allow users to store plotter configurations in nonvolatile memory.

All of the Draftmaster plotters have a maximum pen acceleration of 5.7g and a maximum pen velocity of 43 ips. The plotters' resolution is 0.00025 in. All of the units employ eight pens and work with paper, transparency- and polyester-film, and vellum- and tracing-bond media. The disposable pens feature ceramic tips and an ink regulator that



Sheet-feed, roll-feed, and multiuser with roll-feed models make up the new Draftmaster family of E-size pen plotters that support HP-GL/2.

stops leaks.

The electrostatic plotter family includes the \$45,900 Model 355 Esize color unit, the \$25,900 Model 250 D-size monochrome unit, and the \$29,900 Model 255 E-size monochrome unit. All of the units produce drawings with 406-dpi resolution. A typical plot requires less than a minute to draw. All of the electrostatic units come with the 1-year warranty.

Other features of the electrostatic units consist of an automatic media cutter, a take-up reel for unattended plotting, and front-panel control and monitoring of all the plotter functions. The electrostatic units can create plots with 2048 color or gray-scale lines, and the plotters can merge vector and raster data. Media choices include paper, vellum, and clear and matte film.

The HP-GL/2 language provides

enhancements to the industry-standard HP-GL language. The newer language actually includes fewer commands than HP-GL, but these commands combine with additional parameters and expand the language.

An HP-GL file that requires six minutes to be sent serially from a host to a plotter requires only 1½ minutes when stored in an HP-GL/2 format. The transmission time can be especially important for electrostatic plotters. Raster electrostatic devices must receive an entire vector file before beginning a vector-to-ras-

ter conversion and then producing the plot. HP-GL/2 also provides better control over line characteristics such as width, area fill, image size, and placement.

The electrostatic models are also compatible with a subset of HP's PCL (printer control language) for raster operation. The company's laser, ink-jet, and dot-matrix printers support PCL, and now the electrostatic plotters include similar capabilities. You can also expect to see support for HP-GL/2 in future printer offerings from the company.—Maury Wright

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900.

Circle No. 730

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EDN SPECIAL REPORT

Macintosh-based CAE

Macintosh zealots see the recent flurry of Mac-based CAE/CAD software releases as a torrent of new applications for their beloved system. Skeptics see these releases as too little too late to provide engineers with the depth of alternatives they need for *real* design work. Is the glass half full or half empty?

Michael C Markowitz, Associate Editor

Macintosh fanatics have long pointed to the computer's user interface, the consistency of its applications, and its ability to transfer information across applications as justification for their reverence. But until recently, few CAE/CAD applications would let you design ICs

and pc boards on the Mac.

A number of companies have introduced Macbased CAE/CAD packages since last year's Design Automation Conference. This software runs the price gamut from personal-computer-like \$500 packages to workstationlike \$25,000 packages. These CAE/CAD packages let you perform any function that you can perform on competing workstations. And though many of the vendors of these packages are small startup companies with names such as Bobcat. Dolphin, and Sled, larger well-established compa-

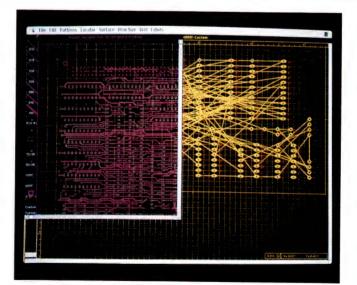
nies such as Data I/O and Schlumberger have also joined such long-time Mac-CAE/CAD developers as Capilano, Design Workshop, Douglas, and Vamp in the Mac attack.

This flurry of software introductions increases the quantity of Mac-based CAE applications to about 50. Contrast this number with the number of applications available for IBM PCs and compatible computers or for Unix-based workstations. According to estimates

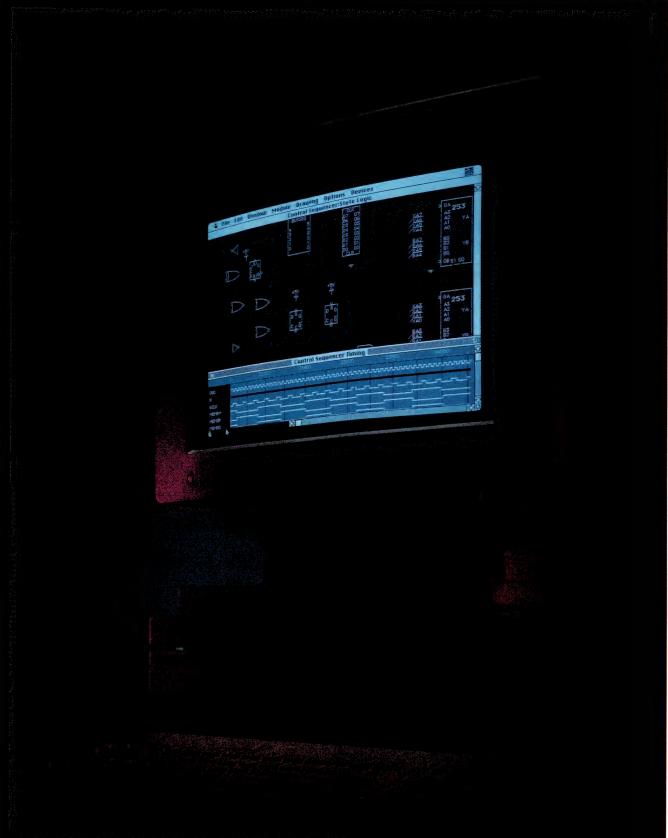
from Dataquest, a San Jose, CA, research firm, IBM PCs and compatible computers offer roughly 300 CAE design applications. Sun Microsystems' June 1989 Portfolio of Electronic Design Automation Software lists 78 vendors, most with multiple offerings. Hewlett-Packard and Apollo workstations run about 95 CAE applications.

Having few choices means that you could be stuck if you're designing a circuit that exceeds the capacity of the CAE/CAD software you're using or requires a capability that your software

doesn't have. Designers apparently understand the limitations implied by the shortage of CAE applications. In a recent EDN survey of engineers and engineering managers who specify CAE/CAD hardware



You can design, layout, and route your pc board using a Mac-based CAE tool from Douglas. Send the company the output files, and you can have finished boards within two weeks.



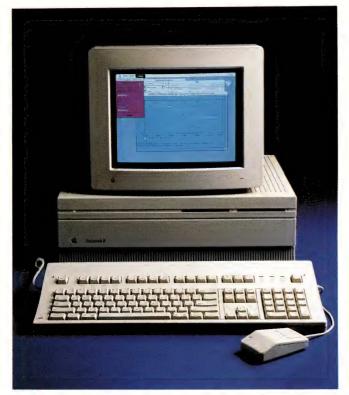
Most Macintosh-based simulation tools let you modify your schematic "on the fly," like this tool from Capilano Computing. As a result, you don't need to exit the simulator, recompile, or even restart your simulation.

According to an EDN survey, there aren't many engineers using the Mac for ECAD, and few engineers are considering using one.

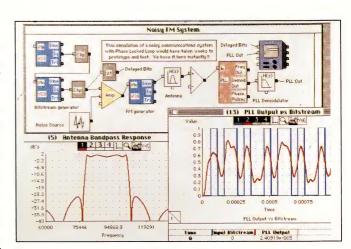
and software, 101 of 134 respondents use IBM PC-based CAE/CAD software, 60 use Unix-based workstations, 8 use a mainframe, and 1 uses a Mac. Some respondents indicated that they use multiple types of computers.

Mac devotees interpret this data to mean that users are waiting for some critical mass of powerful design applications before they adopt the hardware. But accepting this argument presents a Catch-22: Software developers are waiting for user demand before writing applications, but user demand won't develop until these applications exist.

Viewlogic Systems Inc (Marlboro, MA) develops CAE tools for IBM PCs and most workstations—but not for the Macintosh. According to Vice President of Engineering Will Herman, "The Macintosh is a great machine. It would make a terrific system, but the demand just isn't there." Meta-Software (Campbell, CA) Sales Manager Jeffrey Langner and OrCAD Systems' (Hillsboro, OR) John Durbetaki, whose IBM PC-based CAE software has the largest installed base of any CAE software, agree. All three companies say they occasionally get requests for Mac-based software, but



Most of the CAE/CAD applications running on the Mac, like MicroSim's PSpice, let you customize the display's color scheme.



By simulating a system at the block level, you can tweak and tune your design before building a prototype. Imagine That!'s Extend is simulating the output of a digital FM transceiver system locking onto a noisy signal.

they don't think the market justifies the cost of porting their software—yet.

Data I/O recently decided to test the water by porting its Unix-based Abel PLD and PROM design tool to the Macintosh. However, by taking the easy first step—porting to Apple's version of Unix, called A/UX—Data I/O ignored the benefits of the larger installed base of the Mac's Multifinder operating system and its graphical user interface. In January, Data I/O signed an agreement whereby Capilano Computing would integrate the Mac-based Abel, called MacAbel, into Capilano's tools under Multifinder. Although it's no longer actively developing Mac-based software, Data I/O insists that it's still evaluating the Macintosh as a platform for its software.

Some vendors, though, have long supported CAE applications on the Mac. Design Workshop, for example, began developing its DW-2000 IC-layout software about six years ago on a 128k-byte Mac. For founder and Vice President of Engineering Francois Marquis, the Mac's user interface and graphics capabilities were critical to his goal of writing low-cost layout software with the appearance of the ubiquitous Calma layout software.

Similarly, Douglas Electronics' founder and President Chad Pennebaker and programmer Harland Harrison liked the Mac's user interface. Douglas started as a pc-board design house with little computer expertise. The firm originally developed its Mac-based CAE software to let customers adapt Douglas-standard pc boards to customer-specific applications.

John Jacobson is the director of CAD/CAM at Photo-

beam Brookside (Waltham, MA), a small company that offers supplies, performs photoplotting, and fabricates pc boards. Jacobson admits to having been intimidated by computers when he started at Photobeam four years ago. However, his experience with the Mac and earlier versions of Douglas's software has eliminated his fear of working with computers.

Jacobson considers software a 1-sale deal. He reasons that whereas he might only sell one software package to a customer, that customer will only return to Photobeam for other supplies and services if he or she is happy. As a result, Jacobson recommends Mac-based software to computer phobes and Macintosh fanatics, a group he calls Mac-heads. He directs other customers to an IBM PC-based package. Although IBM PC-based software lacks the user friendliness of the Mac software, Jacobson thinks IBM PC-based CAE packages can do more.

Ironically, a vendor of one of the recently introduced Mac-based CAE tools shares some of Jacobson's sentiments. Al Benelli, executive vice president of Bobcat Systems, doesn't think there are many CAE/CAD tools with the potency to design and analyze complex circuits on the Mac. Benelli also says that because workstations are so expensive, engineering departments don't have enough of them. Thus, for every circuit idea you get to develop, another twelve shrivel on the vine for want of a workstation to capture the circuit. He likes the Daisy-, Mentor-, and Valid-based design tools, but thinks those workstations are far too expensive. The problem, according to Benelli, is that most companies don't have enough of these workstations around to give you access to one when you need it. And further, he says, tying up these expensive workstations to do noncompute-intensive schematic capture is foolish.

Capture your design on the Mac

Bobcat's solution to the workstation shortage is transferring the schematic-capture portion of the design cycle to an inexpensive personal computer. The company chose the Macintosh, whose advantage over

Text continued on pg 144

What is a workstation, anyway?

Is a \$10,688 Mac IIci with a 25-MHz 68030 CPU; a 68882 floating-point coprocessor; built-in video circuitry; 8M bytes of RAM; an 80M-byte hard disk; three expansion slots; and eight ports, including a SCSI, a toy or a serious workstation? One way to answer the question is to look at other computers powered by the 68000 μP family. Few would argue that these machines aren't workstations.

The \$8995 HP9000 Model 345 is a 50-MHz 68030-based machine with a 68882 coprocessor. You can upgrade the basic computer with 16M bytes of RAM and a 200M-byte hard disk. The model 345 has one slot for graphics.

Another workstation based on the 68000 CPU family is the Sun-3. A 20-MHz 68030 powers the low-end Sun-3/80, whose price starts at \$5995. You can add a 68881 coprocessor, 16M bytes of RAM, and a hard disk with as much as 1.3G bytes of storage to the basic configuration.

After comparing the hardware, consider the operating systems. Unix supports virtual memory whereas Macintosh's operating system, Multifinder, and MS-DOS don't. Virtual memory enables Unix workstations to appear to have larger memories than they actually do. As it needs information, a CPU running Unix can swap programs and data between physical and virtual memory, which actually resides on the hard disk.

Having virtual memory simplifies true multitasking. Multifinder lets you open multiple windows, each of which represents a separate process. However, be-

cause it doesn't support multitasking, Multifinder can only execute the code in the foreground process. In contrast, Unix's multitasking ability lets you execute code in each of the windows.

Apple does have a version of Unix, called A/UX, which is a true multitasking, multiuser operating system. Unfortunately, only two CAE/CAD packages, MacAbel and MacSilos II, run under A/UX.

So, the Mac is certainly a work-station if you look only at the hardware, but its lack of virtual memory is a bit of an obstacle to running CAE applications. MS-DOS-based applications have a similar impediment. Therefore, from a software perspective, if you consider the IBM PC to be a workstation, then so, too, is the Macintosh.

Some vendors suggest using your workstation for number-crunching applications, such as simulation, and doing schematic capture on the Mac.

Table 1	I-Rep	resentative	Macintosh-based	CAE/CAD	design tools	S
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Company	CAE software	Price	Application	Requirements	Comments
Algorithmic Systems	Ascyn	About \$2000	Logic synthesis	Not available.	Product is available through Capilano Computing.
Bobcat Systems	McLogic	\$2995	Schematic capture	At least a Mac Plus with 512k bytes of RAM. Imagewriter printer.	Tool acts as front end for Daisy, Mentor, and Valid workstations. McBridge translator costs \$4995.
BrainPower Inc	DesignScope	\$250	System simulation	Mac SE or II with 512k bytes of memory.	Performs functional-block system simulations.
BV Engineering	ACNAP	\$350	AC network analysis	Mac SE or II with 512k bytes of memory.	Performs magnitude, phase, and delay calculations. Models may be nested. Does Monte Carlo analysis. 50-node, 200-component limitation. Vendor offers 17 other programs.
CAD/CAM Group	Engineering Capture System	\$2000	Schematic capture	Mac II with 2M bytes of RAM and 20M-byte hard disk recommended.	Capture with physical attributes. Dynamic links to MacSilos II. Database is binary compatible with Sun and IBM PC versions.
Capilano Computing	Design Works	\$685	Schematic capture and simulation	Mac Plus, SE, or II.	Along with schematic capture and simulation, software communicates with word processor, drafting, spreadsheet, database, layout, and other programs.
Data I/O Corp	MacAbel	\$2995	PLD and PROM design	Mac II or IIx running A/UX with 4M bytes of RAM and 80M-byte hard disk.	High-level design-language input to processor that creates programmer load files for PLDs and PROMs. Support and distribution through Capilano Computing.
Design Workshop	DW-2000 Version 3.2	\$10,500	IC layout	Mac II with minimum 2M-byte memory; 5M bytes or more is recommended.	Price includes 1-year service/sup- port and upgrades. Gerber and GDSII compatible.
Deutsch Research	MacSpice and MacSpice Professional	\$995 \$1995	Circuit simulation	Mac II or IIx. 2M to 4M bytes of memory recommended.	Accepts schematics from Capilano Douglas, and Vamp. Measures parameters from waveform plots with a mouse.
Doctor Design	dV/dt	\$595	Timing diagram editor	Not available.	"Timing sketchpad and spread- sheet." Sketches timing diagrams with provisions for propagation delays.
Dolphin Integration	Smash	\$9500	Structural/behavioral simulator	Can run on any Mac. Mac II with color monitor recommended.	Behavioral models use C- compatible language. Spice and Hilo3 compatible.
Douglas Electronics	CAD/CAM Professional System	\$2900	Schematic capture, pc-board layout, and autorouter	Mac SE or II with 512k- byte RAM or more.	Accommodates 50 different view sizes. Options include Gerber File Creator (\$250) and Drill Tape (\$150)
F-Chart Software	FEHT	\$400	Finite-element heat transfer	Mac Plus or larger. Mac II recommended.	Provides numerical solutions to 2-D steady-state and transient con- duction problems. Output via con- tour, flux plots, temperature/ voltage-vs-time plots, and charts.
Formula GmbH	Run (Capture, Layout, and Autorouter)	\$15,600	Schematic capture, pc-board layout, and autorouter	Mac SE or larger with 4M to 8M bytes of RAM.	Capture, layout, and router are modular; they can be purchased separately. Price includes one year's upgrades.

Company	CAE software	Price	Application	Requirements	Comments
Imagine That Inc	Extend	\$495	System simulation for modeling, analysis, and design	Mac Plus, SE, II, Ilx; two 800k-byte floppy drives. Hard drive recommended.	Supports continuous- and discrete event behavioral simulations.
Intusoft	IsSpice/Mac	\$210	Circuit analysis	Any Mac with at least 1M-byte RAM, coprocessor, and hard disk.	Performs dc, ac, transfer function, distortion, and transient analysis. No-coprocessor version, \$95.
MicroCode	CircuitMaker	\$100	Digital capture and simulation	Any Mac with 512k-byte RAM.	Absolute limit of 1800 nodes, though practical limit is 1000 nodes on Mac Plus. Macro library (\$85) and TTL library (\$60).
MicroSim	PSpice	\$1495 \$4950	Circuit simulation	Mac SE with accelerator card or Mac II; 2M bytes of RAM.	Uses 68881 coprocessor. Options include analog behavioral modeling, digital simulation, and device equations.
Momentum Data Systems	MacFilter	\$995	Filter design and analysis	Mac SE or II; coprocessor recommended.	Optional \$200 code generator creates 56001 assembly code.
Nedrud Data Systems	DragonWave	\$1380	Microwave analysis and optimization	Mac Plus or larger.	Draws schematics from 50-elemen library. Software creates node list and calculates noise factor, stability, and group delay.
San Juan Software	MacAC	\$150	Linear capture and simulation	Mac Plus or larger.	Will run on machines without coprocessor. Allows fast modification-resimulation cycles.
Schlumberger CAD/CAM	MacBravo!	\$1950	Capture, waveform editing	Mac II or larger, 5M-byte RAM (8M bytes recom- mended). 40M-byte hard disk.	Direct net-list creation for Spice, Cadat, and Saber simulators. Customizable interface. Compo- nent library costs \$495.
Simucad	MacSilos II	\$5000	Logic and fault simulation	Mac II or larger, 8M-byte RAM and 100M-byte hard-disk recommended.	A/UX version available now. Mac operating-system version due first quarter of 1990.
Sled Systems	Sled	\$25,000	Simulation, syn- thesis, timing analysis, and testability	Mac II, 4M-byte RAM, 80M-byte hard drive, and color monitor recommended.	Hardware-accelerated simulation. Vendor-specific libraries, including quarterly updates, cost \$2000/year.
Sofcad Electronics	Lincad-Mac	\$120	Linear analysis	Mac Plus with 512k-byte RAM.	Interactive analysis tool for as many as 35 nodes.
Spectrum Software	Micro-Cap II	\$895	Schematics and simulation	Mac with at least 512k- byte RAM and an Imagewriter.	Automatically converts your schematic to a net list suitable for simulation. Performs temperature analysis.
Tanner Research Inc	L-Edit	\$1495	IC layout	Mac Plus, SE, and II.	Contains on-line, customizable design-rule checker. Supports MOSIS multiproject wafer program.
Tatum Labs	ECA-2	\$775	Analog-circuit analysis	Any Mac with 512k bytes of RAM.	Has multiple-plot capability. Company also sells thermal-analysis software (\$995) and modeling system (\$2995).
Vamp	McCAD EDS-1 McCAD EDS-2	\$1495 \$1995	Integrated pc-board design packages	Mac Plus or larger, 2M bytes of RAM.	Bundled packages. EDS-1 contains schematics, place and route. EDS-2 adds a digital simulator and behavioral modeling.

EDN March 1, 1990

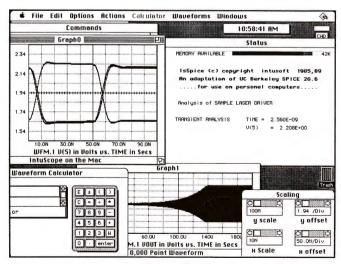
Because of its ability to share data and drawings across applications, the Macintosh is a good tool for you to use in creating your design documentation.

an IBM PC or compatible computer is that the software is friendlier and more amenable to data transfers among different applications.

Using Bobcat's McLogic, you can build your circuit and then transfer it to your Daisy, Mentor, or Valid workstation via Bobcat's McBridge software (\$4995) or using EDIF (electronic design interchange format) over an Ethernet or RS-232C link. The Mac-based front-end schematic-capture tool is compatible with Mac-based software that lets you generate reports, parts lists, and other engineering documents.

Schlumberger shares Bobcat's philosophy that the front-end tool can and should be inexpensive. However, Schlumberger's MacBravo! goes a step further in its utilization of the Mac. Mike Smith, director of channels marketing for Schlumberger, thinks that most designers have already chosen either a proprietary or commercial simulator. MacBravo! acts as a schematic-capture tool and graphical waveform editor. After capturing your circuit and building your stimuli, you can transfer the net list and stimulus files to your workstation for simulation. After the workstation runs the simulation, you can transfer the results back to the MacBravo! software on the Mac for analysis. The company's translation programs get your data back and forth between MacBravo! and your workstation-based simulator.

There are three problems with these companies' approaches. The first is the addition of data translations, which adds another step every time you want to transfer your design between Mac- and workstation-based



With concurrently open windows, IsSpice from Intusoft lets you perform waveform calculations, evaluate node voltages, and change graphic axis scaling.



A personal computer is a workstation when you can connect several together, share files, and work productively using the available software. By this definition, the Apple's Macintosh qualifies as a workstation.

applications. Second, by off-loading the front end of the design process, you just shift the design bottleneck to the simulation and analysis end. In fact, by letting you develop more circuit ideas through schematic capture, you'll have even more circuits competing for limited simulation time on Unix-based workstations. Finally, both approaches assume that engineers have access to a Macintosh.

The issue of an engineer's access to a Macintosh is a consistent thread running through the proMac-CAE/ CAD arguments of most Mac-based-CAE vendors. They claim that engineering departments often have access to many Macintoshes. In some cases, they contend, the secretaries are using these machines. More often, however, Mac-based-software vendors allege that you either share a Mac or have your own machine for documentation. According to Bill Fuchs, Dataguest estimated that in 1988 there were 35,000 Macintoshes in CAD/CAM environments; there was no breakdown of the number in electrical-engineering environments. However, because mechanical, civil, and architectural engineers have had more time to assimilate the Mac, it is safe to assume that electrical-engineering seats account for a small percentage of these machines. Sun Microsystems estimates that of the 200,000 workstations it has sold, between 38,000 and 50,000 are in use in electrical-engineering departments.

Some engineers do use a Mac to generate reports or parts lists, and documentation is where the Mac really shines. In fact, a compelling argument for Mac-

Manufacturers of Macintosh-based CAE/CAD software

For more information on Macintosh-based CAE/CAD packages such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

Algorithmic Systems 399 Pond St No. CS Braintree, MA 02184 (617) 849-0580 Circle No. 650

Bobcat Systems Inc 1607 Raewyck Dr West Chester, PA 19380 (215) 696-2801 Circle No. 651

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The Macintosh's biggest weakness as a workstation is its shortage of CAE/CAD applications.

based CAE/CAD is the Mac's inherent ability to cut information from one application and paste it into another. However, the Mac's advantage in documentation over other personal computers is eroding as Windows on the IBM PC and X/Windows on Unix workstations develop and mature.

One Macintosh user who makes use of the cut-andpaste capability, Dennis Grimm, considers the Macbased Excel spreadsheet one of his most valuable CAE tools. Grimm, a senior design engineer at Radius (San Jose, CA), uses Excel for a variety of tasks. In addition to budgets, his spreadsheet keeps track of signal translations through multiple ribbon cables and worst-case analysis equations.

Grimm is sure that his expectation for the Mac's success as a CAE workstation is no fairy tale. However, you must balance his enthusiasm for the Macintosh as a workstation with the knowledge that Grimm was one of the Mac's original designers. His thoughts typify those of the multitude of Mac-heads, whose allegiance to the Mac borders on fanaticism. These Mac supporters point to the Mac's ability to transfer information across applications as evidence of its ability to integrate engineering functions.

The cut-and-paste feature, however, doesn't guarantee data compatibility across different applications. Like designers trying to interconnect software from different vendors on Unix workstations, Mac users may find that the mix-and-match route is really an obstacle course (Ref 1). Jeff Deutsch of Deutsch Research says, though, that if a developer strictly follows the Mac's application-developer's guidelines, the developer's tools will be interoperable with other tools. Further, he continues, most of the CAE tools developed for the Mac follow those guidelines. Unfortunately, according to Deutsch, many of the tools that developers have ported from other workstations do not.

In addition to Mac-heads, who practically worship the Macintosh, there are also those whose feelings run strongly the other way. These macho elitists look down their noses at the Mac's wimp interface—windows, icons, mice, and pull-down menus are too sissy for them.

Do you like to type?

Bill Dudley doesn't have a problem with "computer weenies who don't like to type." But Dudley, vice president of engineering at Design Computation (Farmingdale, NJ), finds the Mac's graphical user interface nonintuitive. He objects to the "pop-up this,



Although most Mac-based ECAD applications run under Multifinder, Data I/O's MacAbel, a PLD design tool, and Simucad's MacSilos II both run under A/UX.

cutesy that" nature of the GUI. Dudley prefers command-line-driven software for his own use. Recognizing the marketing advantage, though, he has incorporated an optional menu-driven interface into his IBM PC-based CAE products for users who prefer that entry format.

But most people favor graphical user interfaces. In fact, the Mac's reliance on the GUI from the beginning is half of the strategy to which Apple owes much of its success. The GUI makes the machine less intimidating and easier to learn for potential users than command-line-driven software. The interface also makes it easier to relearn a program after you've been away from it for awhile.

The other half of Apple's strategy is attracting potential users early. The company has worked with educators and succeeded in placing many of its Macintoshes in engineering schools. In addition, many Mac-based-CAE/CAD vendors provide educational versions of their software to bring tomorrow's engineers into the Mac camp. As these budding engineers graduate, they may provide some of the user demand necessary to accelerate the development of more numerous and capable Mac-based CAE packages.

Thus, the Mac has a nucleus of devoted users, about 50 CAE/CAD applications, and CAE-competent hardware. What, then, will it take to make the Mac a widely used CAE/CAD platform? First, and of greatest concern to the users, are the applications. Inexpensive software puts CAE/CAD within reach of more engineers, but software vendors must eliminate any perception that the Mac's low-cost software is cheap or

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When you purchase a single-sourced workstation, whether it is a Macintosh, an RT, a Sun-3, a DECstation, or an Apollo/HP machine, you may end up with an orphan.

incapable of doing the job. Too many Mac-CAE/CAD packages are hobbyist programs with limited capabilities. Not enough powerful software exists to let you do your designs today and still provide you with expansion capabilities for the future. There are a few very capable Mac-based CAE/CAD packages and a few more are in the development pipeline, but users need even more.

Secondly, Apple must attract a big-name ECAD software vendor. You could argue that no hardware vendor has ever had to demonstrate the capability of its system before, but unfortunately for Apple and any other latecomers, the rules of the game are different now. Apple's late entrance into the big-time CAE/CAD market and the widespread perception of the Mac as a desktop-publishing computer demands that the company establish its credibility with a well-known CAE/CAD vendor.

Attracting this vendor would help create demand from end users. The history of computers is well documented: Software drives hardware sales. A large CAE-tool vendor would stimulate demand, which would entice other CAE-tool developers to write engineering packages for the Mac. A larger base of applications would create the highly competitive and dynamic market conditions that exist with other workstations.

Finally, Apple must demonstrate its commitment to the Macintosh as a workstation. Last year, Mentor Graphics publicly trumpeted Apple Computer's purchase of workstations for schematic capture and simulation, concurrent-fault simulation, and pc-board layout



Most Mac-based CAE tools were written specifically for the Mac, but some, such as L-Edit from Tanner Research, were converted from MS-DOS.

as the "largest single order in EDA (electronic design automation) history." You wouldn't expect to hear about DEC or Sun buying another vendor's workstations to design its next-generation machines. Proclamations like this one send the not-so-subtle message that either the Mac itself or the CAE tools running on the Mac aren't sophisticated enough for the Apple to do the job.

In addition, users want to see a hardware-upgrade path. Some Mac-software vendors say the Mac IIci is a 4.5-MIP machine; users want to know when they can expect a 10-MIP version. Or a 20-MIP system. Unixworkstation vendors have been almost doubling the performance of their machines every nine months. Competitive pressures have forced IBM PC and compatible-computer vendors to upgrade their machines as fast as Intel can shrink the 80386 and 80486 CPUs. Users have to wonder if Apple is under the same pressures to upgrade its machines.

Tom Weishaar, publisher of the Apple II newsletter A2-Central, voices still another concern. Weishaar believes Apple has never succeeded at structuring itself as a multiproduct vendor. In the past, according to Weishaar, Apple has supported the Apple II, the Apple III, the Lisa, and the Mac—but never more than one at a time. And today, he says, the Mac is Apple's one product. As evidence, he points to Apple's failure to introduce any significant new Apple IIs since the September 1986 rollout of the Apple IIgs. Also, the company doesn't offer the file-system-translation modules that would let Apple II users read Mac disks, although Weishaar expects this feature in Apple's next operating-system upgrade.

Weishaar warns that when Apple develops its next-generation hardware, the company may cast Mac users adrift. Mac users will find the same lack of commitment, research-and-development funding, and support that Apple II users get now, he alleges. And, he points out, because Apple vigorously prevents others from copying its hardware, the company's enthusiastic support is essential for support from software developers. Once Apple's enthusiasm for a particular computer architecture wanes, third-party support of that architecture could easily dry up, as Weishaar contends it has for the Apple II.

Executives at Apple deny Weishaar's allegations about lack of support. Nancy Stark, product manager for the Apple II product line, offered the evolution from the II+, the IIe, the IIc, and the IIgs as evidence of Apple's support of the Apple II since its introduction



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in 1979. And since the introduction of the IIgs, Apple has provided upgrades that have included an upgraded operating system, an enhanced IIc Plus, a 1M-byte Hgs, and a video overlay card. Finally, she said, "Apple will continue to sell, service, and support the Apple II product line as well as work with third-party developers to provide Apple II customers with the solutions that they require."

Weishaar's concerns were for the Mac, but be aware that any time you consider a sole-sourced computer, the manufacturer could leave you with an orphan. However, Weishaar's concerns are particularly meaningful given reports that Apple is considering developing a Motorola 88000-based workstation (Refs 2 and 3). According to RISC Software: Strategies, Directions, Markets, published by the Information Network, "The development of a RISC-based workstation is on hold until the company (Apple) decides how it could market a completely new line of computers, marked by an operating system that is incompatible with its other models."

Apple would neither confirm nor deny the existence of an 88000-based development effort. According to spokesperson Nancy Morrison, the company has a policy not to discuss products that aren't available.

Despite Weishaar's concerns and other weaknesses in Apple's Mac-as-a-CAE/CAD-platform strategy, you can use the Macintosh and its available software to capture and analyze most of your circuits. And-especially if you aren't in a hurry to buy a workstation and software anytime soon—you might want to keep the Mac in mind. Kirk Shorte, Apple's electronic design applications manager, recognizes most of the Mac workstation's shortcomings and is working to address and correct each of them.

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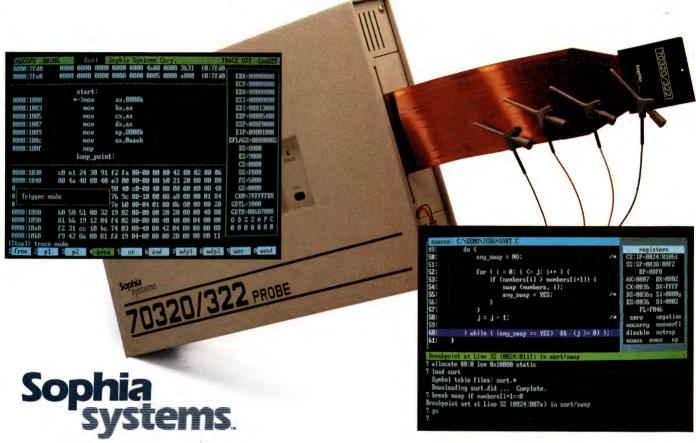
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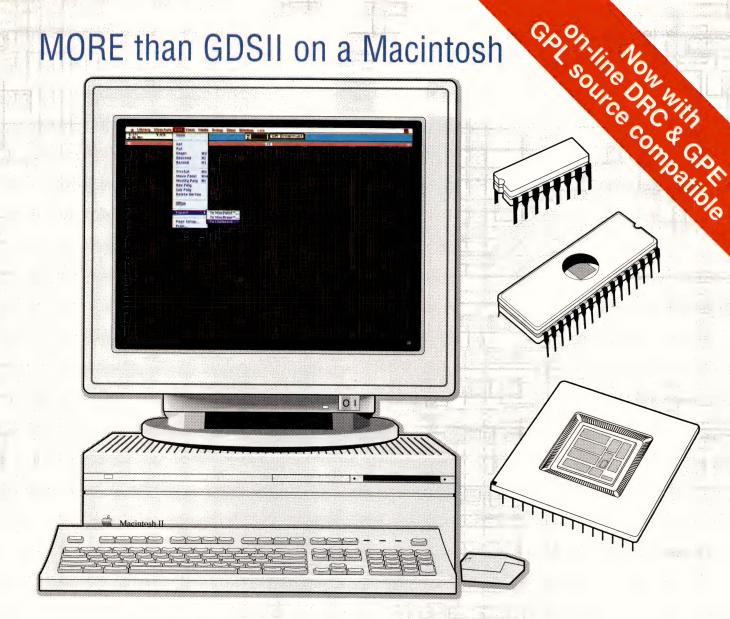
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Spice-compatible op-amp macromodels Part 2

Op-amp macromodel proves superior in high-frequency regions

Part 1 of this article pointed out some deficiencies of the existing Boyle op-amp macromodel and described the structure of a new, modular macromodel for use with Spice-compatible circuit simulators. Part 2 describes the practical implementation, using the new structure, of models for two recent op amps; provides sample Spice net lists; and compares the simulation accuracy and computation time of the new models with those of the Boyle approach.

Mark Alexander and Derek F Bowers, Precision Monolithics Inc

Because the main goal of the new structure is to provide improved ac accuracy, the model must also correctly represent the common-mode behavior. So, the modeling team selected the PMI OP-42, a JFET-input op amp, as its first guinea pig, largely because the Boyle model cannot properly accommodate a JFET input stage. Although the team had to work out all the equations pertaining to the JFET input stage before they could test the complete model, this stage turned out to be fairly easy to handle mathematically and did not hinder the development of the final macromodel structure.

Fig 1 shows the resulting implementation. The physical OP-42 has a gain-bandwidth product of approximately 10 MHz and a symmetrical slew rate of

 $50V/\mu sec.$ The CMRR-versus-frequency curve of this amplifier indicates that a zero at about 100 kHz is necessary in the model's common-mode gain stage.

Listing 1 shows the net list for the OP-42 macro-model, which has 8 poles, 2 zeros, plus a zero in the common-mode gain stage at 100 kHz. The model of even a relatively stable amplifier needs that many poles and zeros in order to accurately mimic the gain and phase behavior of the physical device at high frequencies.

Inspection of the output-stage section of the net list shows that the open-loop output resistance is 45Ω . A 250-nH inductor, connected in series with the output terminal, compensates for the rise in effective open-loop output impedance at high frequencies. The current-limiting network formed by diodes D_3 and D_4 and voltage sources V_4 and V_5 clamps the maximum output current at approximately ± 30 mA.

Simulation-accuracy comparisons

Fig 2 shows the gain and phase response of a physical OP-42 connected as an inverting, unity-gain amplifier that has $1\text{-k}\Omega$ input and feedback resistors and runs from $\pm 15\mathrm{V}$ supplies. You can see a small amount of peaking (about 2 dB) in the closed-loop-gain curve, and the phase shift increases rapidly above 2 MHz. Figs 3a and 3b show the gain and phase response of the new OP-42 macromodel under the same conditions. The gain response shows the same amount of closed-loop peaking as that of the real circuit; the phase response almost

EDN March 1, 1990

Both the Boyle and the new configurations model an op-amp output stage as a perfectly symmetrical voltage source.

exactly matches that of the real device to at least 10 MHz.

Figs 4a and 4b, which show the corresponding output curves from the Boyle implementation, clearly demonstrate the deficiencies in the Boyle model's response accuracy. The gain response does not show the 2-dB peak, indicates too steep a roll-off, and is quite inaccurate above 10 MHz. The Boyle model's phase

response does not even come close to the real circuit's response. The OP-42 macromodel, with its multiple pole/zero complement, emulates the ac response of the actual circuit more accurately.

Fig 5 shows the measured transient response of the inverting, unity-gain OP-42 amplifier with a 430-pF capacitive load. For a 400-mV peak-to-peak input signal, there is about 75% overshoot and 100% under-

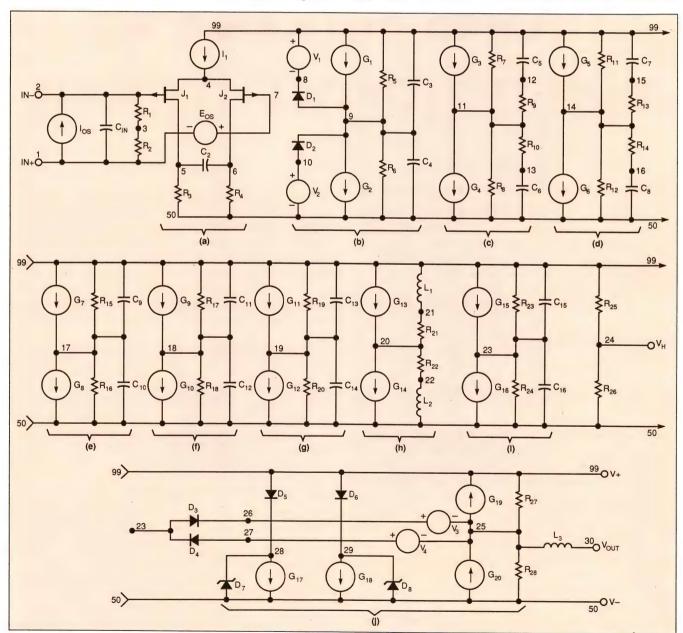


Fig 1—The OP-42 macromodel is more complex than its Boyle counterpart, requires more time for simulation, but pays off in greatly improved accuracy.

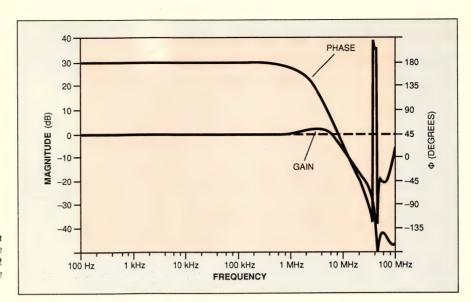


Fig 2—When you connect the OP-42 in a unity-gain, inverting configuration the gain response shows a slight peak at about 6 MHz; there is a rapid increase in phase shift above 2 MHz.

```
Listing 1—OP-42 SPICE macromodel net list
OP-42 MACROMODEL
                                                                      * POLE AT 53 MHz
.subckt OP-42 1 2 30 99 50
                                                                      r17
                                                                            18
                                                                                 99
                                                                                          1E6
                                                                                          1E6
                                                                      r18
                                                                            18
                                                                                 50
                                                                                 99
                                                                                          3E-15
*INPUT STAGE & POLE AT 15.9 MHz
                                                                      c11
                                                                            18
                                                                                          3E-15
                                                                      c12
                                                                            18
                                                                                 50
                                                                                              24
                                                                                                    1E-6
                   5E11
                                                                      g9
r1
                                                                      g10
                                                                            18
                                                                                 50
                                                                                          24
                                                                                              17
                                                                                                    1E-6
r2
                   5E11
r3
     5
          50
                   707.36
                                                                      * POLE AT 53 MHz
r4
     6
          50
                   707.36
cin
     1
          2
                   5E-12
                   7.08E-12
                                                                      r19
                                                                            19
                                                                                          1E6
c2
il
     99
                   1E-3
                                                                      r20
                                                                            19
                                                                                 50
                                                                                          1E6
ios
                   4E-12
                                                                      c13
                                                                            19
                                                                                 99
                                                                                          3E-15
eos
     7
                   poly(1)
                             20
                                  24
                                      1E-3
                                                                      c14
                                                                            19
                                                                                 50
                                                                                          3E-15
                                                                                          18
                                                                                              24
                                                                                                    1E-6
j1
j2
     5
              4
                   iχ
                                                                      q11
                                                                            99
                                                                                 19
                                                                                                    1E-6
                                                                            19
                                                                                 50
                                                                                              18
     6
                   iх
                                                                      q12
                                                                        COMMON-MODE GAIN NETWORK WITH ZERO AT 100kHz
  GAIN STAGE & POLE AT 45 Hz
                                                                                          1E6
                                                                      r21
                                                                            20
                                                                                 21
r5
          99
                   176.84E6
                                                                            20
                                                                                 22
                                                                                          1E6
                   176.84E6
                                                                      r22
r6
          50
                                                                            21
                                                                                 99
                                                                                          1.5915
С3
          99
                   20E-12
                                                                       11
C4
          50
                   20E-12
                                                                      12
                                                                            22
                                                                                 50
                                                                                          1.5915
                                                                                                    1E-11
g1
     99
          9
                   poly(1)
                                       3.96E-3
                                                 1.4137E-3
                                                                      g13
                                                                            99
                                                                                 20
                                                                                          3
                                                                                              24
                   poly(1)
                                                                                          24
                                                                                               3
                                                                                                    1E-11
g2
     9
          50
                              6
                                       3.96E-3
                                                 1.4137E-3
                                                                      g14
                                                                            20
                                                                                 50
     99
v1
          8
                   2.5
v2
     10
          50
                   3.1
                                                                       * POLE AT 79.6 MHz
d1
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     10
          9
                   dx
                                                                      r23
                                                                                 99
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                                                                                          1E6
                                                                            23
  POLE-ZERO PAIR AT 1.80 MHz/2.20 MHz
                                                                      c15
                                                                                 99
                                                                                          2E-15
                                                                            23
                                                                                          2E-15
                                                                      c16
                                                                                 50
                                                                                                    1E-6
r7
                   1E6
                                                                      g15
                                                                            99
                                                                                 23
          50
                                                                      g16
                                                                            23
                                                                                 50
                                                                                          24
                                                                                               19
                                                                                                    1E-6
r8
                   1E6
r9
      11
          12
                   4.5E6
                                                                       * OUTPUT STAGE
r10
     11
          13
                   4.5E6
C5
     12
          99
                   16.1E-15
     13
                   16.1E-15
                                                                       r25
                                                                                          111.1E3
c6
          50
      99
                                                                      r26
                                                                            24
                                                                                 50
                                                                                          111.1E3
g3
                                                                            25
                                                                                          90
g4
     11
          50
                   24 9
                            1E-6
                                                                      r27
                                                                                 99
                                                                            25
                                                                                          90
                                                                                 50
                                                                       r28
                                                                       13
                                                                                          2.5E-7
* POLE-ZERO PAIR AT 1.80 MHz/2.20 MHz
                                                                            28
29
                                                                       g17
                                                                                 50
                                                                                          23
                                                                                              25
                                                                                                    11.1111E-3
                                                                                               23
                                                                                                     11.1111E-3
                                                                                          25
r11
                   1E6
                                                                       g18
                                                                                 50
                                                                      g19
                                                                            25
                                                                                 99
                                                                                          99
                                                                                               23
                                                                                                     11.1111E-3
r12
     14
          50
                   1E6
                                                                            50
                                                                                 25
                                                                                                     11.1111E-3
                                                                       g20
r13
     14
          15
                   4.5E6
                                                                            26
                                                                                 25
27
                                                                                          0.7
          16
                   4.5E6
r14
      14
                                                                            25
          99
                                                                       V4
                                                                                          0.7
c7
      15
                   16.1E-15
                                                                       d3
                                                                            23
                                                                                 26
                                                                                          dx
c8
      16
          50
                   16.1E-15
                                                                       d4
                       24
11
                                                                                 23
                                                                                          dx
g5
      99
          14
                   11
                              1E-6
                                                                       d5
                                                                            99
                                                                                 28
                                                                                          dx
      14
          50
                              1E-6
g6
                   24
                                                                       d6
                                                                            99
                                                                                 29
                                                                                          dx
                                                                                          dy
                                                                            50
                                                                                 28
* POLE AT 53 MHz
                                                                       d7
                                                                       d8
                                                                                 29
                                                                                          dŷ
                                                                            50
r15
                   1E6
          99
                                                                       * MODELS USED
      17
          50
                   1E6
r16
c9
          99
                    3E-15
      17
                                                                       .model jx PJF(BETA=999.3E-6 VTO=-2.000 IS=4E-11)
c10
      17
          -50
                   3E-15
                                                                       .model dx D(IS=1E-15)
g7
      99
          17
                   14
                       2.4
                              1E-6
                                                                       .model dy
                                                                                    d(IS=1E-15 BV=50)
g8
*
      17
          50
                        14
                              1E-6
                                                                       .ends OP-42
```

Though more accurate than the Boyle model, the new macromodel runs more slowly because of the larger number of circuit elements.

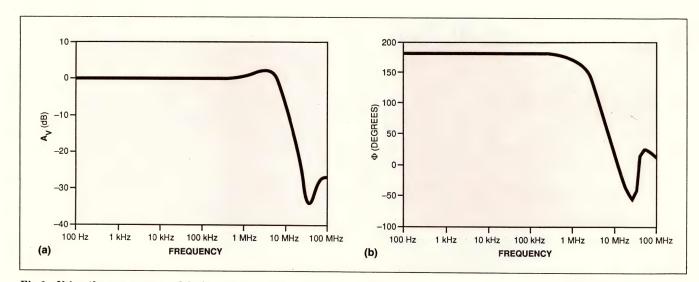


Fig 3—Using the new macromodel, the simulated gain response (a) of the OP-42 is very like that of the real device, with a slight peak at 4 MHz. The phase-response accuracy (b) is very good. This curve closely follows that of the real device.

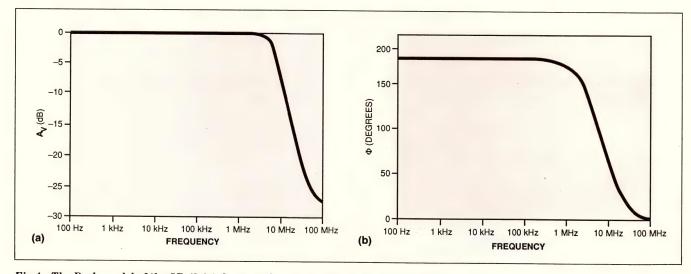


Fig 4—The Boyle model of the OP-42 (a) does not show the amplitude peak at 4 MHz that is characteristic of the real device. The phase response (b) also is not very accurate, especially in the region beyond 10 MHz.

shoot. The simulation results from the new macromodel (Fig 6) show about 115% of both overshoot and undershoot. This simulated value is quite close to the actual value on the negative half of the waveform but differs from the actual value on the positive half. The explanation for this anomaly is that although the new macromodel has a perfectly symmetrical output stage, the op amp being modeled may not. The OP-42, in fact, has an asymmetrical, all-npn-transistor output stage; as a result, the high-frequency, open-loop response is variable and depends on whether the output stage is sinking or sourcing current.

The Boyle configuration, too, models an op amp's output stage as a perfectly symmetrical voltage source and, as Fig 7 shows, it incorrectly simulates the undershoot on the negative half of the output waveform. It does come reasonably close on the positive half, but the ringing frequency is lower than that of the real circuit.

This inability to model nonsymmetrical output-stage behavior is inherent in the Boyle approach and is still, unfortunately, shared by the new macromodel. However, it is a drawback that you can work around. If, during the model-generation process, you find that the

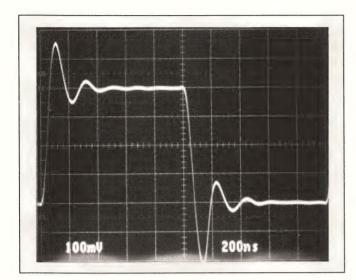


Fig 5—An OP-42 with a 430-pF capacitive load shows both overshoot and undershoot when driven with a 500-kHz, 200-mV-peak square wave.

overshoot is different from the undershoot, you should use the larger of the two values in calculations pertaining to the output inductor. Then with capacitive loads, the inductor value will yield the worst-case overshoot and undershoot results.

Execution-time comparisons

Assuming that no convergence problems exist in the macromodel, the time taken for Spice to produce an operating-point calculation or a dc-transfer curve is largely a function of the number of circuit elements specified in the net list. Consequently, the new OP-42 macromodel was almost exactly twice as slow as its Boyle counterpart and required 2.27 times as many iterations to reach the final solution. Similar remarks apply to the ac-analysis case, where the run-time overhead of the new macromodel was almost exactly twice that of the Boyle macromodel. However, the two models required about the same number of iterations for ac-response simulation.

Evaluating the computational overhead for a transient analysis is quite difficult, because of the large number of factors involved. In particular, the new macromodel will exhibit considerably more detail than the Boyle model. The simulator must therefore use a much finer time step and perform correspondingly more calculations. However, the large number of ideal elements in the model results in a very good probability of convergence. Therefore, you can sometimes speed up the analysis by allowing more iterations per time step, a

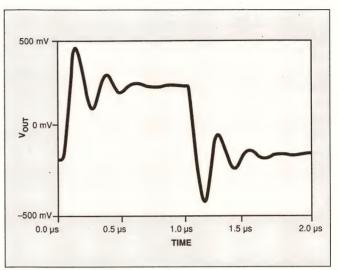


Fig 6—The new macromodel's simulation of an OP-42 with a capacitive load of 430 pF shows the symmetrical nature of the model's output stage.

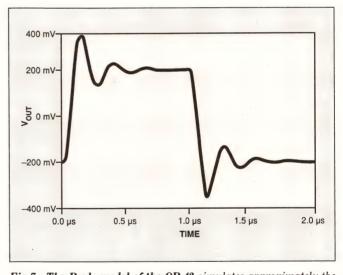


Fig 7—The Boyle model of the OP-42 simulates approximately the right amount of overshoot, but its ringing frequency is too high.

procedure which often allows the simulator to maintain a coarser time step and reduces the number of backtracks.

Most Spice simulators default the number of transient iterations to 10. You can override this default by setting ITL4 to a larger number (say 40) in the .OPTIONS section. Additionally, relaxing RELTOL to 0.01 (the default value is usually 0.001) will also speed up the run time by slightly reducing the accuracy. This reduction is quite permissible because the macromodel is only an approximation anyway. Note,

The large number of ideal elements in the new macromodel increases the probability of convergence and may let you speed up the simulation process.

however, that Figs 6 and 7 were generated with REL-TOL set to 0.001 rather than 0.01, so that the curves would be more accurate. Another way of speeding up the transient analysis is to use GEAR rather than TRAPEZOIDAL integration; however, such integration can generate results that appear considerably less oscillatory than they actually should be.

Using 0.01 for RELTOL, 40 for ITL4 and trapezoidal integration, the OP-42 macromodel proved to be 3.64 times slower on transient runs than the Boyle model

and required 2.15 times as many iterations. The reduction in simulation speed, though large, is acceptable, and is outweighed by the advantage of greatly improved accuracy.

The OP-61 macromodel

The OP-61 is a bipolar-input, wide-band, precision op amp that typically has a gain-bandwidth product of 200 MHz (at a test frequency of 1 MHz) and a slew rate of 40V/µsec. The model of this device (Fig 8) is

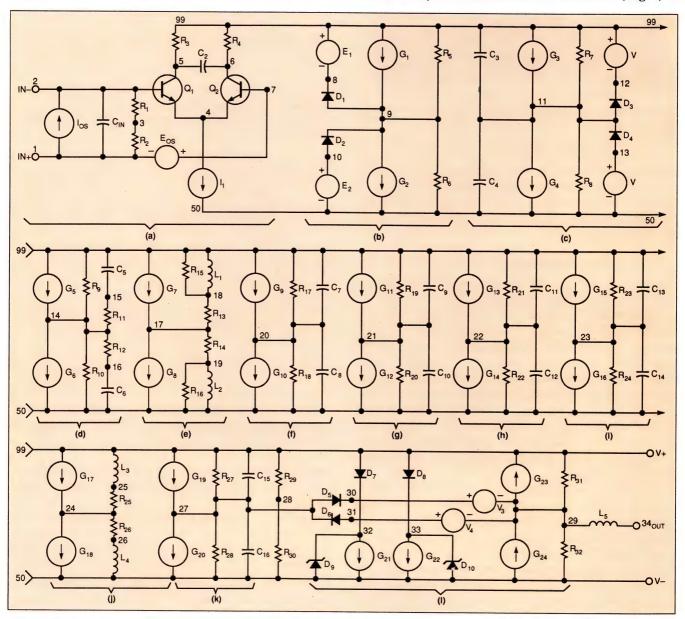


Fig 8—The model schematic of the OP-61 looks similar to that of the OP-42, except that it has an additional gain stage.

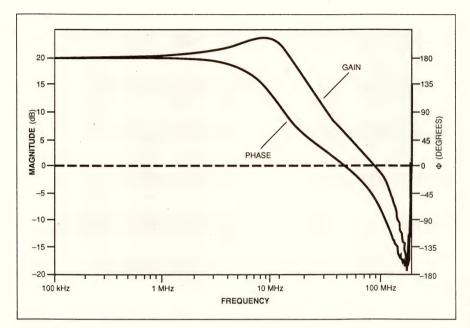


Fig 9—When you connect a real OP-61 as an inverting amplifier with a gain of 10, the gain response shows a 3-dB peak at 10 MHz.

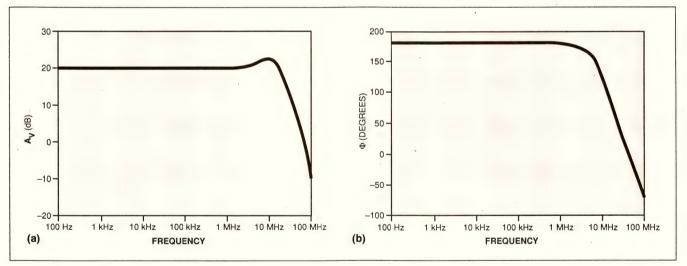


Fig 10—The simulated gain (a) of the OP-61 macromodel shows the correct amount of peaking at 10 MHz. Further, its phase response (b) at 40 MHz differs by only 10° from that of the real device.

only slightly more complicated than that of the OP-42. The OP-61's common-mode rejection starts to roll off at a lower frequency than the CMRR of the OP-42, but at 1 MHz it is still a respectable 80 dB. The net list (**Listing 2**) indicates that the OP-61 model requires 9 poles and 2 zeros to mimic the open-loop frequency response, and a common-mode gain of zero at 40 kHz.

Notice that this model has an additional gain stage (stage b in Fig 8) between the differential input stage and the main gain stage (c, Fig 8), which generates the dominant amplifier pole. The extra gain stage is

necessary in this particular model because the OP-61 does not satisfy the limiting equation, which relates the slew rate, open-loop gain, and the dominant pole frequency for the bipolar input stage (see box, "Calculation of model parameters," in Part 1). The OP-61 model requires an open-loop gain of 100 dB and slew rate of $40V/\mu sec$, but the gain-bandwidth product (and hence the dominant pole frequency) is too high to allow a single stage to generate all of the open-loop voltage gain.

Therefore, this model uses two gain stages, which

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Accurate predictions of a new device's performance help avoid design errors that would be expensive to correct at the manufacturing stage.

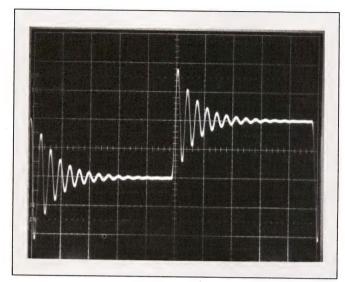


Fig 11—The transient response of a real OP-61, when connected as an inverting amplifier with a gain of 10 and a capacitive load of 207 pF, shows some asymmetry. The input signal is a 500-kHz square wave with a peak amplitude of 10 mV. The vertical scale is $0.1V/\mathrm{div}$, and the horizontal scale is $0.2~\mu\mathrm{sec/div}$.

together give the requisite 100 dB of gain. The first gain stage has a gain of 200; the second has a gain of 500. You have to provide clamping in the first gain stage, in order to limit the maximum drive voltage applied to the voltage-controlled current sources in the second gain stage. This clamping action then limits the amount of peak current delivered to the compensation capacitors C_5 and C_6 , and thus limits the maximum dV/dt in the second gain stage.

The first gain stage must provide a fair amount of gain, because the maximum differential output voltage of the input stage is only 51.6 mV. To facilitate clamping with voltage sources and diodes, you need a much larger voltage. A gain of 200 in the first gain stage would result in an unclamped voltage of $\pm\,10.32V$ relative to V_h during slewing, but the clamping circuit limits this to approximately $\pm\,5.0V$ regardless of the rail voltages. This configuration allows reliable clamping action even when the power-supply voltages are as low as $\pm\,4.4V$. It also results in the desired slew rate of $40V/\mu sec$.

Simulation-accuracy comparisons

Fig 9 shows the measured gain and phase responses of a physical OP-61 configured as an inverting amplifier with a gain of 10. Here, a 1-k Ω feedback resistor, a 100Ω input resistor, and $\pm 15\mathrm{V}$ power supplies were used. The amplitude response exhibits a definite peak

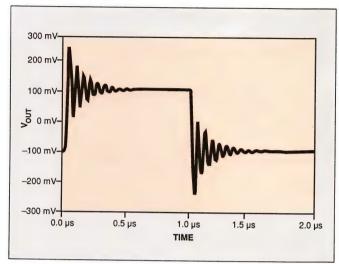


Fig 12—The simulated transient response of the OP-61 macromodel quite closely matches the transient response of the real device.

of about 3 dB in the 10-MHz region, and the phase shift also increases quite rapidly above 10 MHz. The corresponding responses of the new macromodel (Figs 10a and 10b) show excellent conformance to the measured gain response of the OP-61. The gain curve exhibits the requisite gain peak of slightly over 2 dB just above 10 MHz. The phase-response accuracy is also quite good; the error is only about 10 degrees at 40 MHz, and is probably within the range of variation one would expect to see on a breadboard because of parasitic capacitances and other physical effects. This new macromodel is therefore a useful tool in predicting the performance of the OP-61, even before you evaluate a breadboard.

Fig 11 shows the transient response of the OP-61, which might appear to be rather unstable until you notice that the device is driving a 207-pF capacitive load. The waveform exhibits some asymmetry between the amounts of overshoot and undershoot (180% versus 220%), but the OP-61, like the OP-42, does not have a perfectly balanced output-stage structure. The choice of the output inductor (L5 in the model) largely determines how closely the simulated transient response will mimic the real response. In fact, the simulation (Fig 12) yields symmetrical overshoot and undershoot of about 150%, which is a little low, and a ringing frequency which is a little high, compared to those of Fig 11. This discrepancy is unlikely to be of much importance to the user; if it is important, however, you could easily bring the simulated response closer to that of the real device by slightly increasing the

Listing 2—OP-61 SPICE macromodel net list

r13 17 18 r14 17 19 r15 18 99 r16 19 50 11 18 99 12 19 17 g8 17 50 * * POLE AT 40 MHz * POLE 20 50 c7 20 99 c8 20 50 g90 50 g10 20 50 *	SECOND 7 11 8 11 3 11 4 11 3 99 4 11 3 99 4 11 1 11 4 13 7 11 4 13 7 11 1 14 1 14 1 11 1 14 1 11 1 14 1 11 1 14 1 11 1 14 1 11 1 14 1 11 1 14 1 11 1 14 1 11 1 14 1 11 1 14 1 11 1 14 1 11 1 14 1 11 1 14 1 14 1 11 1 14	ACROMODE OP-61 1 STAGE & 3 99 99 2 6 6 7 4 7 4 9 50 50 50 6 8
1E6 2.529E6 2.529E6 1.342E-3 1.342E-3 1.42E-3 14 28 11E-6 28 14 1E-6 1E6 1E6 1E6 3.979E-15 3.979E-15 3.979E-15 17 28 11E-6 28 17 1E-6	A STITT A GGSSALITE & G	POLE AT 300 MHz 5E11 5E11 51.6 51.6 51.41E-12 5.141E-12 1E-3 2E-7 poly(1) 24 28 400E-6 1 qx qx AGE 1E6 1E6 1E6 1E6 1E6 1E6 1E6 1E6 1E7 1E8

* MODE * .model .model .model	*10 *10 *10 *10 *10 *10 *10 *10	# COMM # COMM # COMM # 25 2 126 2 113 2 114 2 114 2 117 9 114 2 117 9 117 9 118 2 118 2 119 1 119 1 1 1 1	POL 22 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2
gx NPN(dx D(op-61	300 30 11 17 10 10 10 10 10 10 10 10 10 10 10 10 10	3 50 9 23 9 23 50 0N-MODE 4 26 4 26 4 26 5 99 6 50 9 24 4 50 7 99 7 99 7 99 7 99 7 99 7 99 7 99 7 9	AT 200 1 99 1 50 1 50 9 21 1 50 9 21 2 50 2 50 2 50 2 50 2 70 2 70 2 70 2 70 2 70 2 70 2 70 2 7
BF=1250) IS=1E-15) IS=1E-15 BV=50)	20.0E3 20.0E3 30 30 1.65E-7 29 27 29 27 33.333E-3 29 27 33.3333E-3 6.2 6.2 6.2 6.2 6.2 6.2 6.2 6.2 6.2 6.2	GAIN 1E 11E 11E 11E 11E 11E 128 288	E6 E6 796E-1 0 2E: 10 2E: 8 20 E6 E6 E6 E6 E6 E6 E6 E6 E6 E6 E6 E6 E6

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Today's emphasis in modeling is on improving simulation accuracy rather than on shaving every possible second from the execution time.

value of the output inductor.

You can get some feeling for the performance of the new OP-61 model by comparing it to that of the OP-42 (no Boyle model of the OP-61 exists). For the dc bias point calculation, the OP-61 macromodel was faster than the OP-42 macromodel; for ac-response simulation, however, the OP-61 macromodel was slower by a factor of 1.18.

In the transient response simulations, the OP-61 macromodel took 1.76 times as long as the OP-42 macromodel and needed 1.56 times as many iterations. In this connection you should remember that the simulation time of a transient run increases as the output becomes more oscillatory. Therefore, a direct comparison of the OP-42 and OP-61 execution times is not exactly fair, because the OP-42's response is less oscillatory than that of the OP-61.

Simulation goals are changing

The goal of any computer model is to accurately model some physical phenomenon; the more complex the phenomenon, the longer the time required for the computer to perform the necessary calculations. The goal of the Boyle op-amp model was to reduce the number of nonlinear elements that required simulation, and hence to decrease the run time to an acceptable value. The Boyle model was not created with ultimate accuracy in mind, but it could correctly predict the low-frequency performance of an op amp, and was satisfactory for the relatively low-performance devices of its day.

Today, however, there is more and more demand for ever higher performance, and accurate prediction of a new device's performance can help to avoid design errors that would be expensive to correct at the manufacturing stage. Thus, accurate modeling of the highfrequency performance is essential, and in that region the Boyle model is inadequate. The improved op-amp macromodel described here not only models the highfrequency response and transient behavior of an op amp much more accurately than the Boyle model, but also does not need too much more CPU time to do its job. Today, with powerful desktop workstations available, the emphasis in modeling is on improving simulation accuracy rather than shaving every last bit from the execution times. The new macromodel is thus a good compromise.

The single most limiting factor of this new macromodel is that, for Spice compatibility, the model must be written in the form of a net list with real circuit elements. Some new simulators (such as Saber, from Analogy Inc) allow you to define models in a specialized programming language that eliminates circuit-type constructs. The Saber modeling language, known as Mast, is very similar to C and allows powerful manipulation of internal variables. This feature would allow the output stage of the new macromodel, for example, to be completely described mathematically. A Saber model simply would not need all of the diodes and additional sources that the Spice model requires for output-stage current correction. The defining equations for the output stage would directly take into account any load current that was being drawn from the model's output terminal. It is very likely that the new macromodel will be implemented in Saber at some time in the near future.

Authors' biographies

Derek F Bowers is staff vice-president of design at Precision Monolithics Inc, where he has worked for 11 years. He has been closely involved in the development of a wide variety of analog devices, including op amps, reference sources, and D/A and A/D converters. Derek holds a BSC in physics and mathematics from the University of Sheffield, England. In his spare time he enjoys music and brewing.



Mark Alexander has for nearly two years been a staff design engineer at Precision Monolithics Inc, where he is working on the design and development of digital-audio products that have not yet been announced. He holds a BASc (EE) from the University of Toronto, Canada. In his spare time he enjoys the design and construction of audio equipment, cooking, and walking. He is also a knowledgeable collector of antique watches.



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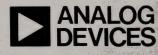


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Build testable ASICs using nonstructured design techniques

Due to the perceived penalties of designing for testability, designers often ignore the testability of their ASICs until late in the design phase. However, if you use nonstructured—as opposed to formal—design-fortest techniques, you can limit the risk of building untestable chips and improve the quality of your ASICs.

Daniel J Payne, Silicon Compiler Systems Corp

ASIC designs that do not address testability often incur unnecessary testing costs. These designs also suffer from poor reliability in the field and can require an inordinate amount of fault-simulation time. Circuits not designed for test are also more likely to suffer from overruns in engineering design time. Furthermore, if you ignore testability, your circuit may suffer other ills. Little could be worse than to have your system-critical ASIC pass all of the manufacturing tests and still fail in operation due to a manufacturing flaw.

Before considering ways to achieve high testability, consider the trade-offs you might incur when incorporating design-for-test techniques. First, the cost of testability will be different for every circuit and is dependent on the architecture of the design and how you approach testability. Also, as you add logic to improve testability, your circuit paths may become longer, and longer delay paths correspond to slower operating speeds.

However, two things will help you overcome most testability problems. First, address the testability questions of a design in a methodical manner. Second, have high-level testability tools at your disposal. If these testability tools let you use informal design-fortest techniques that don't limit your design flexibility, so much the better. And, if you know how to recognize logic blocks that are not testable and can transform them into testable logic blocks, then your ASIC designs will be more reliable. Further, with tools such as automatic test-pattern-generation (ATPG) software, you can reduce testing costs.

Test-pattern-generation software creates a compact set of production test vectors and provides testability and fault-grade-analysis reports. A major benefit of ATPG is the reduction of on-chip test hardware. Limiting this chip hardware minimizes speed degradation, power consumption, and the silicon area and I/O counts that tend to soar with the proliferation of test hardware.

Before using the ATPG software, you need to define your testability game plan. You can divide design-fortest techniques into two classifications: structured and nonstructured. A structured design-for-test technique

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Nonstructured design-for-test techniques are loosely defined and less restrictive than structured techniques.

is a hardware test method that you universally apply to a design (Ref 1). For example, level-sensitive scan design (LSSD) is a structured design-for-test technique because its rules dictate that you use level-sensitive scan latches for all sequential elements in a design and that you connect them in a predetermined fashion. Full scan is also a structured technique. Full scan requires that you use multiplexed scan flip-flops for all the flip-flops in your ASIC design and that you connect them in a shift-register fashion. Another structured method is the built-in logic block observer (BILBO) technique (Ref 2). This technique requires that you have an internal circuit that stimulates the internal nodes of a design and another internal circuit that validates the final result through signature analysis.

Nonstructured design-for-test techniques include any combination of hardware schemes that allow for increased coverage of the potential manufacturing faults in an ASIC circuit. For example, a multiplexer that connects the output of a difficult-to-detect node to an I/O pin of an ASIC circuit is a nonstructured

design-for-test technique. Partial scan is a nonstructured technique that requires only some of the flip-flops in the design to be scan-path flip-flops. You should choose the flip-flops for a partial-scan path on the basis of the observability and controllability of the internal ASIC nodes. Addressable latches or flip-flops are also nonstructured design-for-test techniques.

You can apply all of the aforementioned methods to any ASIC design. However, the trade-offs between the level of testability that you achieve with each method and the method's overall effect on cost and performance will vary with each design. A strict level-sensitive-scan-design approach, although comprehensive, may not be the most efficient method for many designs. Although noted for their high fault coverage, BILBO techniques may add considerable silicon area and increase the machine cycle time of the system. When you universally apply structured techniques to a design, they can require as much as a 20% increase in silicon area and increases in I/O count, power, and packaging size. Nonstructured techniques can allow

An algorithm for minimizing test vectors

ATPG programs typically handle combinational logic well because the logic's outputs are a direct function of the inputs. Sequential circuits, however, present a more difficult problem for these programs due to the circuits' time dependency. Many ATPG programs overcome the test-vector generation problem of sequential logic by restricting the storage elements that you can use. Other programs convert all the sequential logic in a design to time-dependent combinational logic. This technique is called time unrolling.

Another concept important to pattern generation is sequential depth. This depth is the number of clock cycles an input signal takes to propagate through to the circuit's output. With some ATPG software, you can set the sequential depth as an input vari-

able. Setting the sequential depth too low causes the software to give up too soon; setting it too high lets the CPU run on.

To time-unroll a circuit, consider as an example a sequential circuit over a restricted time. For

the duration of this time, the ATPG program translates a sequential circuit into a combinational equivalent. Imagine, for example, that you have a circuit schematic on a piece of paper. Make many copies and stack

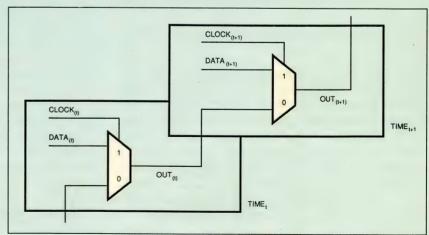


Fig A—A technique called time unrolling lets you model a level-sensitive latch as a pair of multiplexors viewed with a strobe light.

for high testability with as little as 1% extra silicon area.

To gain the full advantage of nonstructured designfor-test techniques, you should understand controllability and observability. The more controllable and observable a logic block's internal nodes are, the easier
it is to test the block. Controllability is a measure of
how well you can control the inputs of a logic block
from the input of an ASIC. For example, an ASIC's
input pin that connects directly to the input pin of a
logic block has the highest level of controllability. On
the other hand, a node deeply embedded within an
ASIC might have a low level of controllability or,
worse, may not be controllable at all. The difficulty of
controlling the logic level is due to the many levels of
gating from the input pins.

If you can observe the logic level of an internal node of an ASIC at an output pin, the node has a high level of observability. In contrast, a node buried deep inside an ASIC may have a very low level of observability. In general, however, it is often difficult to make a quick visual determination of a node's controllability and observability from a schematic.

Because testability is a function of both controllability and observability, there are ways for you to assess the testability of different types of logic blocks. As a rule, logic blocks without feedback are testable. Pure combinational logic without feedback is an example of testable logic because combinational logic normally exhibits a high level of controllability. On the other hand, circuits containing feedback exhibit poor testability resulting from the difficulty of propagating a fault on a feedback node to the output. PLA state machines and modulo counters often exhibit poor testability due to their feedback paths. Because memory circuits such as RAM and ROM are usually embedded deep inside an ASIC and require very large sets of input stimulus and output observation test vectors, they are also difficult to test. A final example of a hard-to-test logic block is the ripple counter, since it requires 2^N·MDNM/vectors to propagate a fault from an input to the output, where N is the number of stages.

them up. The position of a copy in the stack corresponds to a time, and each page corresponds to the state of the circuit at that time. There are now N copies of each signal, and each copy has its own logic state. There is no logical connection between pages except via circuit elements that store state.

Consider the level-sensitive latch in Fig A. The latch has two inputs: Clock and Data. If Clock is a logic 1, then the latch copies Data to its output. However, if Clock is a logic 0, then the latch copies its previous output value to the current output. Therefore, you can translate the latch into a 2-input multiplexer via the following equation:

 $OUTPUT_{(t+1)} = CLOCK_{(t+1)} \cdot IN_{(t+1)} + CLOCK_{(t)} \cdot OUTPUT_{(t)}.$

After performing a similar operation on all elements that store state, you'll have a 3-D schematic with only combinational elements. This simplification allows for the inclusion of automatic test-pattern generation for sequential circuits.

After performing sequentialto-combinational logic conversion, the ATPG algorithm searches for the nodes that are most controllable and observable. The search for controllable nodes is called justification; the search for observable nodes is called sensitization. After determining which nodes are controllable and observable, the ATPG software finds the sensitization and justification paths that have the highest number of nodes. The software then generates vectors for these groups of paths to produce a minimum set of test vectors that will uncover a maximum number of faults.

Both time unrolling and concurrent justification and sensitization have two goals. First, these techniques aim for a minimized test vector set with maximized fault coverage. Their secondary goal is to minimize CPU time. These algorithms, along with a bottom-up ATPG design-for-test methodology, let you run ATPG software programs on workstations without an accelerator and without consuming large blocks of CPU time.

To ensure your ability to detect processing faults, all of the nodes in your circuit should be controllable and observable.

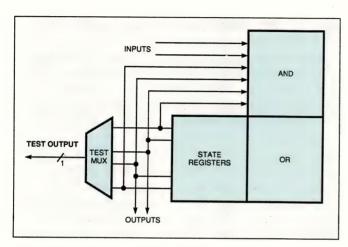


Fig 1—You can increase the testability of PLA-based state machines with feedback paths by multiplexing the feedback paths and the normal I/O signals to the periphery.

To increase the testability of logic blocks that feature poor observability and controllability, you can use several nonstructured design methods. For PLA-based state machines (Fig 1), connect feedback nodes through a multiplexer to the periphery of the ASIC. For RAM and ROM, use a test counter that sequences through the address space of the memory. For the memory's outputs, you can use a parity tree with a linear feedback shift register (LFSR). This register is a pseudorandom-pattern generator that you can use to generate stimulus and compress logic test results into a short, consistent signature (Fig 2). As long as

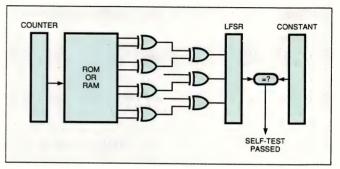


Fig 2—With a linear-feedback shift register, you can compress the test results from a logic block, a memory in this case, and compare them to a known-correct value.

there aren't any manufacturing faults on your ASIC, the signature should duplicate a standard value stored either on the ASIC or in the system.

You can make ripple counters testable by breaking them into several sub-blocks (Figs 3a and 3b). Subdividing the counters reduces the number of vectors that you need to control or observe the circuit because you only have to simulate smaller portions of the circuit.

Whether you use structured or nonstructured techniques, there are two types of logic blocks. Some logic blocks are easy to test, whereas others exhibit poor testability or, worse, are untestable. Circuits that exhibit poor testability have several common characteristics. One characteristic is that it is impossible to generate a test-vector set that can uncover IC manufacturing faults modeled as stuck-at-1 and stuck-at-0. For these

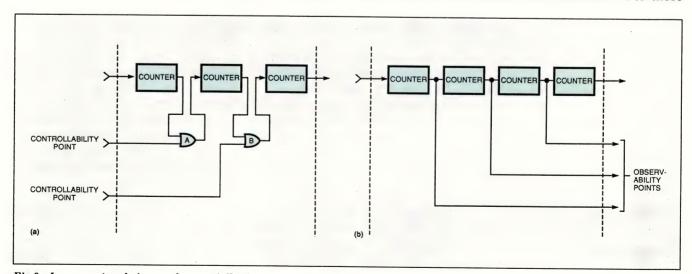


Fig 3—Long counter chains can be especially time consuming to test unless you break the counters into smaller blocks with appropriate controllability and observability points.

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Test patterns generated with ATPG software don't guarantee that your ASIC will work in the target system; they do guarantee that the ASIC is built as you designed it.

untestable circuits, no quantity of vectors will constitute an exhaustive test, and the fault coverage for any given set of test vectors will be low. Another characteristic of poor-testability logic blocks is that they require an inordinate number of test vectors to detect the associated manufacturing faults.

Besides the actual logic-block design, another element that contributes to the testability of your ASIC is your ability to create a test-vector set that will achieve a high fault-grade level. Even though a test-vector set that results in a high level of fault grading for your circuit may exist, finding this test set may be difficult and time consuming. In these cases, automatic test-pattern generators, testability-analysis programs, and fault-grade programs can help.

Design-for-testability methodologies

ATPG offers you several routes to ASIC testability. However, depending on which path you choose, the time you spend to achieve testability will vary. One ATPG method is to design the entire ASIC and then use ATPG software. The software then generates a set of test vectors for maximum fault coverage. Afterwards, you can add vectors or hardware to improve the fault coverage. Although this passive design-fortest approach is viable and you may achieve fault coverage better than 95%, it often does not fully fault-test critical portions of a design. The entire ASIC may have 95% fault grading, but specific critical blocks of the design may have much lower fault-grade levels. Further, such an approach may often result in higher levels of CPU runtime.

Using a bottom-up approach with ATPG, you can achieve a higher level of fault grading and assure fault grading of critical portions of your design. When following this approach, you run each sub-block of an ASIC design through the pattern generator individually. By using ATPG software at the lowest levels of the chip hierarchy first, you identify logic blocks whose fault coverage is poor early in the design process. You can then rerun the software each step up the hierarchy. After you construct the entire circuit, you then rerun the ATPG program on the entire design (Fig 4).

The major advantage to the bottom-up approach is that it lets you assess the testability of each block before you embed the block in the circuit. This evaluation lets you redesign a nontestable block for testability at an early stage, which keeps testability problems from multiplying. A nontestable block may not only

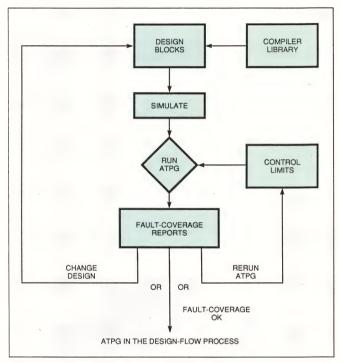


Fig 4—A well-thought-out design methodology, including automatic test-program generation, is one of the best weapons in assuring a testable ASIC.

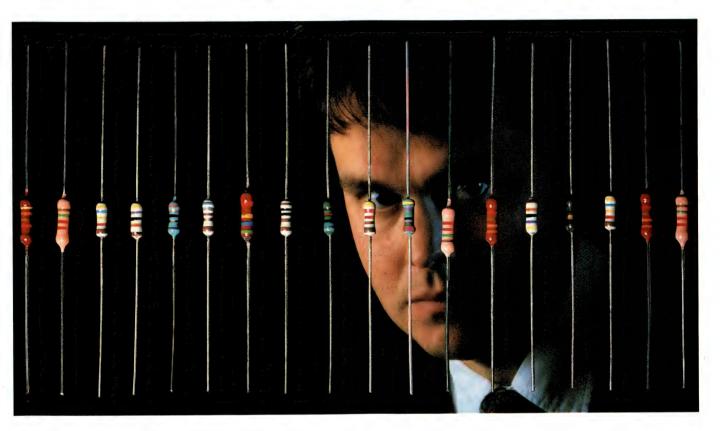
have local undetectable faults but may also prevent other portions of the design from achieving testability. Further, if you keep nontestable logic blocks out of the design, the final pattern-generating pass will run faster and produce a more efficient set of test vectors.

The ATPG algorithm with fault grading is an N³·MDNM/ problem—as the circuit complexity doubles, the CPU time increases by a factor of eight. To minimize this CPU time, try a divide-and-conquer approach, which is consistent with the bottom-up approach. Partition the circuit into two or more smaller pieces and then run ATPG software on each piece. Dividing a large circuit into N small ones and using multiple ATPG runs makes the total CPU time equal to the sum of each run plus the set-up time for each subcircuit.

When designing ASICs for testability, it is critical that you be able to locate nodes that have poor controllability, poor observability, or undetected faults. With this knowledge, you can add circuitry to increase either the observability or controllability of the node, thus making a successful fault-grade vector possible.

To examine how ATPG improves the testability of

A lot of buyers are still in the dark



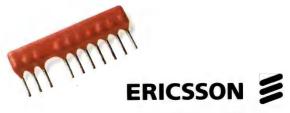
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Ericson Components AB S-164 81 Kista-Stockholm, Sweden Telephone + 46 8 757 5000 Telefax + 46 8 757 4413 A bottom-up approach with ATPG software lets you assess and improve the testability of embedded subcircuits before you bury them deeper into your ASIC.

a design, consider a DSP circuit of about 30,000 gates with 88 input pins, 45 output pins, and 24 power pins. The DSP circuit consists of several building blocks: adders, multiplexors, multipliers, a register file, shift registers, random logic gates, a barrel shifter, and incrementor blocks. After analyzing the design, you decide that two partial-scan rings would improve the testability of the design. Since the scan rings require less than 5% of the silicon in the design, partial scan can be both an efficient and cost-effective approach to higher fault coverage.

After creating and running simulation patterns, you can run ATPG software on the DSP design using one of two criteria to end the program. You can specify either a CPU time limit or a percent fault-coverage target. Some ATPG packages use heuristic analysis to decide that fault coverage cannot be further improved.

One problem that frustrates some ATPG programs is sequential logic (see box, "An algorithm for minimizing test vectors"). Using a time-unrolling technique with a small sequential depth, you can produce an initial set of vectors with 70% fault coverage. You can then use these vectors as initialization vectors for a second ATPG run during which you increase the sequential depth to improve the fault coverage. (In the DSP example, this second ATPG run used 94 CPU hours on a Sun 3/260 platform to generate 95.8% fault coverage using 473 vectors.)

Some ATPG programs complement nonstructured design-for-testability techniques by providing test patterns for both combinational and sequential logic. These programs allow high fault coverage with a minimum number of test vectors. This efficiency permits full-scan fault-coverage levels without full-scan test hardware. ATPG programs also provide a list of nodes that are difficult to test. With this list, you can determine where to place testability hardware to increase fault coverage. Further, since ATPG generates a minimal set of test vectors with maximum fault coverage, the software reduces the design time required to generate high-fault-coverage test vectors.

Using ATPG with nonstructured design-for-testability techniques is a viable testability solution for complex designs. Nonstructured design-for-test methods such as partial scan and ATPG offer you a way to increase the testability of an ASIC design. The price you pay for this testability is only a small increase in

silicon area and I/O counts. This approach offers a significant advantage over full-scan techniques, which can increase the ASIC's die area and require additional designer hours.

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Author's biography

Daniel Payne works in Silicon Compiler Systems' technical marketing department where he creates CAE/CAD demos, trains field applications engineers, and specifies features to add to future software revisions. He is a graduate of the University of Minnesota engineering program and a past chairman of the Monterey Bay subsection of the IEEE. Daniel enjoys reading, 18th century music, and spending time with his wife and three children.



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WHAT'S COMING IN EDN

EDN Magazine's March 15, 1990, issue will feature a staff-written Special Report on how analog switchers and multiplexers save pc-board space and increase your signal-switching options. The issue will also kick off EDN's All-Star PC project with a discussion of the groundwork done to put the PC together. A third staff-written report will focus on how mathematical software packages can ease problem solving.

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LTC1052	Single, 7652 Upgrade	5 µ V	0.05µV/°C	1.5 <i>µ</i> Vp-p	Yes	± 9V
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TOUGH PRODUCTS FOR TOUGH APPLICATIONS.

EDITED BY ANNE WATSON SWAGER

PLD adds flexibility to motor controller

V Lakshminarayanan Centre for Development of Telematics Bangalore, India

The stepper-motor controller shown in Fig 1 uses no discrete devices and is flexible enough that you can program it for any type of drive. The circuit uses a PLD to generate the necessary logic sequence depending on the type of drive you're using. This PLD approach improves upon the shift-register and up/down counter logic-sequencing generation methods because spurious noise pulses can't alter the drive sequence. In the counter and shift-register methods, a single change caused by noise in any bit can continually circu-

late in the logic and alter the drive sequence completely. Using a PLD also adds flexibility to the sequencing logic design.

The 74273 octal D flip flop latches the PLD outputs at the required frequency. The XR-2013, a high-voltage, high-current Darlington transistor array, translates the output logic level of the octal latch to a higher voltage. You can apply voltages as high as 50V to each phase of the stepper motor in order to force the required current through the motor winding. Each Darlington pair in the array can supply 600 mA on a continuous basis, which is sufficient phase current to drive a small stepper motor. To drive large stepper motors, you can increase the drive-current-per-phase by paral-

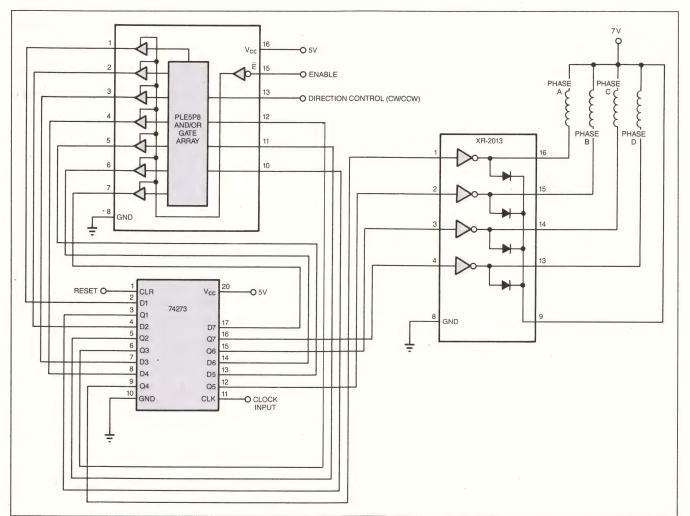


Fig 1—This 3-chip stepper-motor controller requires no discrete components, and you can attain any type of drive by suitably programming the PLD.

EDN March 1, 1990

leling two or more of the Darlington pairs in series with each phase's winding.

The circuit uses the PLE5P8 PLD, which has five inputs and eight outputs. The circuit uses three of the five inputs for the state-incrementing control function. Another input controls the motor's direction input. The circuit uses three of the eight outputs to generate the next address, and four of the outputs to drive the four motor phases. The circuit doesn't require that you connect any external free-wheeling diodes across the phase windings because they are included in the XR-2013.

Table 1 lists the timing generator programming details for different types of stepper-motor drivers. The variable P represents the direction control bit (clockwise vs counterclockwise), and the variables A through D represent the four motor phases. You can derive the PLD programming equations shown in Table 2, using Karnaugh maps. Table 2 presents the programming details for the PLD for some of the commonly used drive sequences.

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A2 A1 A0	B2 B1 BØ				Jonitro	ier (iming generator
;STATE ;AAA ;210	NEXT STA				SIGNA		; COMMENTS
LLL LLH LHL LHH	LLH LHL LHH HLL	L L L	H L L	L H L L	Location Location	L L L H	
LLL LLH LHL LHH	LLH LHL LHH HLL	H (200) H (400) H (400)	H L L	L H L L	L CONTRACTOR	L L L	;PHASE A ON WAVE- ;PHASE B ON DRIVE ;PHASE C ON CCW ;PHASE D ON DIR.
LLL LHL LHL	LLH LHL LHH HLL	L	H L L	H H L L	L H H	L L H	;PHASE A ON TWO- ;PHASE B ON PHASE ;PHASE C ON DRIVE ;PHASE D ON CW DI
LLL LHL LHH	LLH LHL LHH HLL	H 200 H 200 H 300	H L L L L L L L L L L L L L L L L L L L	H H L L	L H H	L L H	;PHASE A ON TWO- ;PHASE B ON PHASE ;PHASE C ON DRIVE ;PHASE D ON CW DI
LLL LLH LHL HLL HLH HHL HHL	LLH LHL LHH HLL HLH HHL HHH LLL	L L L L L L	H L L L L H	L H H H L L L	L L H H H L L	L L L H H	;PHASE A ON HYBRI ;PHASES A,B ON DRI ;PHASE B ON CW DI ;PHASES B,C ON ;PHASE C ON ;PHASES C,D ON ;PHASE D ON ;PHASES A,D ON
LLL LHL LHL HLL HHL HHL HHL	LLH LHL HLL HLH HHL HHL HHH	H H H H H H	H H L L L L	L H H H L L L	L L H H H L L	L L L L H H	; PHASE A ON HYBRI ; PHASES A, B ON DRI ; PHASE B ON CCW DI ; PHASES B, C ON ; PHASE C ON ; PHASES C, D ON ; PHASE D ON ; PHASES A, D ON

Table 2—PLD equations

```
WAVE DRIVE
```

NEXT STATE GENERATOR

B2= /A2*A1*AØ

B1 = /A2*A1*/AØ + /A2*/A1*AØ

BØ= /A2*/AØ

STEPPING SEQUENCE GENERATOR

A = /A2*A1*AØ*P + /A2*/A1*/AØ*/P

B = /A2*A1*/AØ*P + /A2*/A1*AØ*/P

C = /A2*A1*/AØ*/P + /A2*/A1*AØ*P

D = /A2*/A1*/AØ*P + /A2*A1*AØ*/P

TWO-PHASE DRIVE

NEXT STATE GENERATOR

B2= /A2*A1*AØ

B1 = /A2*A1*/AØ + /A2*/A1*AØ

BØ = /A2*/AØ

STEPPING SEQUENCE GENERATOR

A = /A2*/A1*/AØ + /A2*A1*AØ

B = /A2*A1*P + /A2*/A1*/P

C = /A2*A1*/AØ + /A2*/A1*AØ

D = /A2*A1*/P + /A2*/A1*P

HYBRID DRIVE

NEXT STATE GENERATOR

B2 = A2*/AØ + A2*/A1 + /A2*A1*AØ

B1= AØ :+: A1

BØ= /AØ

STEPPING SEQUENCE GENERATOR

A = /A2*/A1*/P + /A2*/A1*/AØ + A2*A1*P + A2*A1*AØ

B = /A2*AØ*/P + /A2*A1*/P + A2*/AØ*P + A2*/A1*P

C = A2*/A1*/P + A2*/A1*/AØ + /A2*A1*P + /A2*A1*AØ

D = A2*A1*P + A2*A0*P + A2*A1*/P + A2*A0*/P

EDN March 1, 1990

Frame-grabber PLL integrates controller

Luis de Sa and Vitor Silva University of Coimbra, Coimbra, Portugal

The frame-grabber PLL circuit shown in Fig 1 includes a CRT controller that performs both address generation and frequency division. The 6845 can implement additional functions, such as the definition of an active display window, and the switching between different video norms without additional logic. Host software must synchronize the CRT controller with the video signal during the initialization process by applying a

pulse to the reset input of the CRT controller after detecting the beginning of an even field. This host-assisted operation, which only needs to occur once, clears the 6845 internal-address counter and leaves intact the contents of the other registers.

The LM1881 video-sync separator extracts two synchronization signals from the video-signal input. By using appropriate buffering, you can use the host CPU to read the O/E Field signal. The second sync signal output of the LM1881 is the composite sync signal, which carries both horizontal and vertical information.

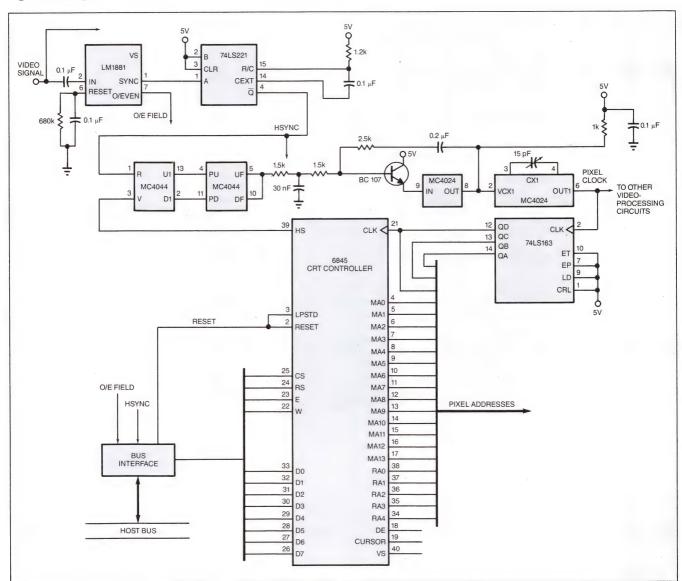
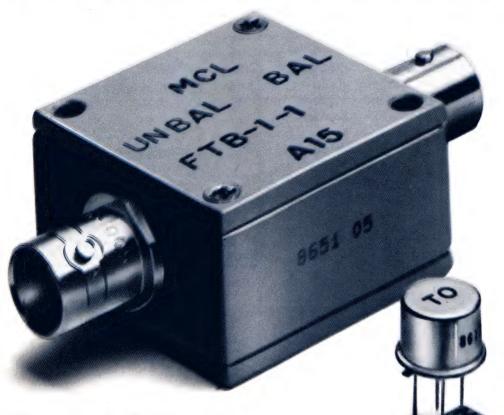


Fig 1—This frame-grabber circuit includes a 6845 CRT controller, which acts as a programmable divider inside the loop of a PLL frequency synthesizer.

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EDN March 1, 1990 CIRCLE NO. 102 181

The 74LS221 removes serration pulses to avoid disturbing the PLL during the vertical retrace period. Thus, pin 1 of the MC4044 phase-frequency detector receives a clean horizontal sync signal.

You should adjust the variable capacitor between pins 3 and 4 of the MC4024 VCO so that it free runs at 12.5 MHz for the NTSC standard or 14.8 MHz for the CCIR standard. If you set the VCO frequency to 13.6 MHz the PLL will lock to either 12.5 or 14.8 MHz, giving the software sole control to switch between video standards. You should take care to decouple the 5V line near the VCO. It's imperative that no power-supply noise reach the input at pin 2. Otherwise, your clock frequency will wander.

The 74LS163 4-bit counter divides the pixel clock by 8 and generates the three least-significant addresses for the 6845's memory. The pixel frequency is further divided by the 6845 so that the HS output of the controller equals the line frequency, thereby closing the PLL loop.

The C program shown in **Listing 1** assumes that the 6845's controller's physical address is $1C0000_{HEX}$, and it's 8-bit read/write control register's address is 180001_{HEX} . The 18-byte NTCS array contains the values necessary to program the 6845 for a 512×480 -pixel resolution under the American TV standard. For the European standard, you can program the 512×512 -pixel resolution with the values in the CCIR array.

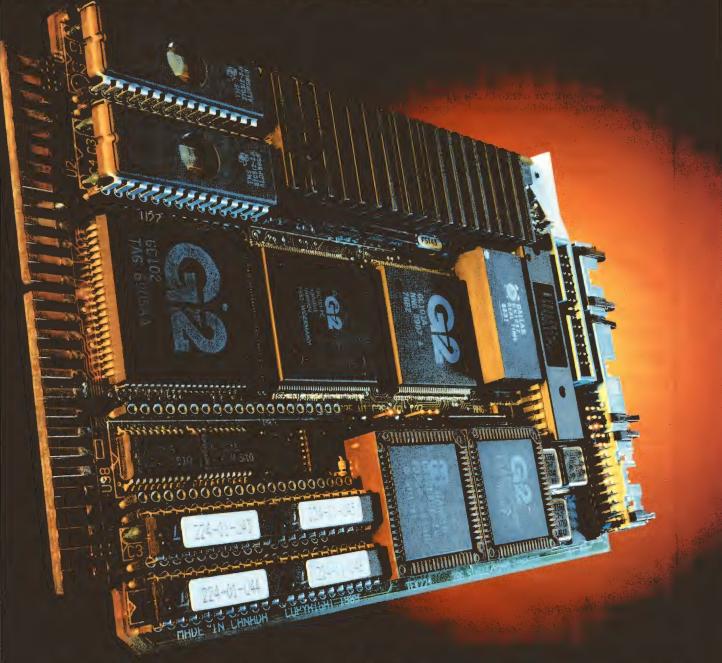
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Listing 1-6845 controller program

```
# DEFINE CRT ADDR OX1C0001L
                         /* Address of CRT address register*/
# DEFINE CRT DATA OX1C0003L
                         /* Address of CRT data register */
                         /* Address of status/control req. */
# DEFINE STAT REG OX180001L
# DEFINE MASKO O
# DEFINE MASK1 1
# DEFINE MASK2 2
# DEFINE NTCS OFF 18
# DEFINE CCIR OFF 33
MAIN()
 REG BYTE *POINT1, *POINT2;
                          BYTE i;
/* First put 6845 reset line at logical one */
 POINT1 = STAT REG; /* Point to status/control register */
 *POINT1 = MASK1;
/* Program CRT registers for NTCS operation */
 POINT1 = CRT ADDR; POINT2 = CRT DATA; I = 0;
 WHILE ( I \leq \overline{17} )
     /* Detect falling edge of odd/even field signal and apply
after 18 ( 33 for the European system)
                                 horizontal lines */
 POINT1 = STAT REG; I =1;
 WHILE (!(*POINT1 & MASK1));
                              WHILE ( (*POINT1 & MASK1) );
 WHILE ( I <= NTCS OFF )
     WHILE ( !(*POINT1 & MASK2) ); WHILE ( (*POINT1 & MASK2) );
     ++I;
 *POINT1 = MASKO;
                  *POINT1 = MASK1;
}
```

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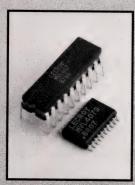
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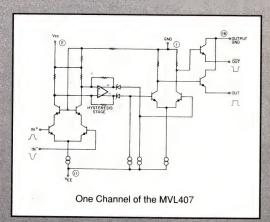
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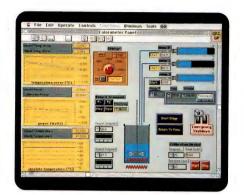
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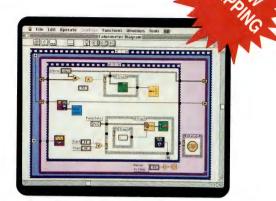
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Gould Inc, 3631 Perkins Ave, Cleveland, OH 44114. Phone (216) 361-3315. Circle No. 352

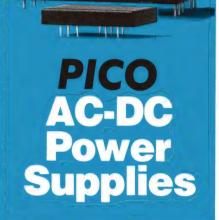


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or segment the RAM to capture multiple short events. The internal 80286 processor can operate as an IBM PC-compatible computer with third-party software. You can configure the unit with different channel modules and controller peripherals. \$13,275. Delivery from stock to 90 days.

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Softaid Inc, 8930 Rte 108, Columbia, MD 21405. Phone (800) 433-8812; in MD, (301) 964-8455. FAX 301-596-1852. TWX 640-265-2092.

Circle No. 354

Diagnostic Module

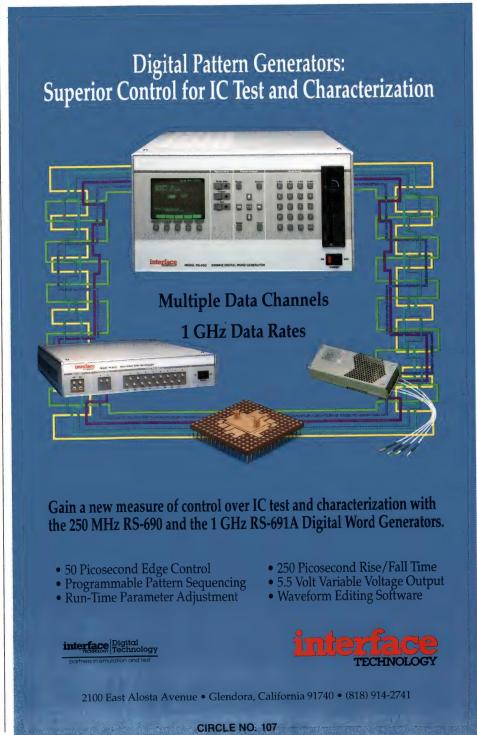
- Tests IBM PC and compatible mother boards
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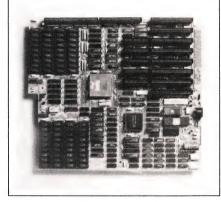
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Tallgrass Technologies, 11100 W 82nd St, Overland Park, KS 66214. Phone (913) 492-6002. FAX 913-492-2465. Circle No. 356



- Has a burst-mode, interleave memory architecture
- Has an IBM PC/AT footprint with compatible mounting holes The Excell 486-25 is a mother board with a 25-MHz Intel 80486 µP. The CPU contains an internal 8k-byte



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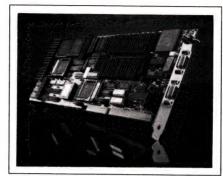
supports either 4M or 8M bytes of 100-nsec dynamic RAM (DRAM). The board can accommodate both static-column and fast-page DRAM. \$3995. (100).

Commax Technologies Inc, 2031 Concourse Dr, San Jose, CA 95131. Phone (408) 435-5000. FAX 408-435-5005. Circle No. 357

Display Controller Board

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- 4M bytes of display-list RAM can run AutoCAD 386 programs

Designed for the 16-bit ISA bus, the 550 display controller can display 256 simultaneous colors from a palette of 16.7 million for noninterlaced monitors with either 1280×1024 — or 1024×768 -pixel resolution. The controller can also operate in dual-screen mode or single-screen mode via a VGA (Video



Graphics Adapter) pass-through connector. The board comes with 4M bytes of display-list RAM, which can handle large drawing sizes requiring extended memory, such as those for AutoCAD 386. The RAM is expandable to 8M bytes. Operating with the Xenix and extended-DOS operating systems, the board comes with Hydra software, which reads 3-D wireframes directly from a hard disk produced under AutoCAD or VersaCAD. An additional program,

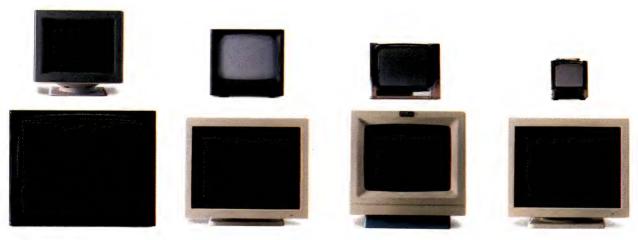
Nth View, makes drawing-slide files accessible locally, over a network, or from a modem at a remote site. 1024×768 -pixel version, \$4995; 1280×1024 -pixel version, \$5995.

Nth Graphics Ltd, 1807-S W Braker Lane, Austin, TX 78758. Phone (800) 624-7552; in TX, (512) 832-1944. Circle No. 358

VMEbus CPU Board

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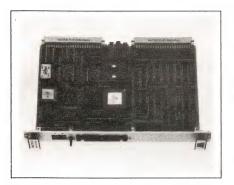
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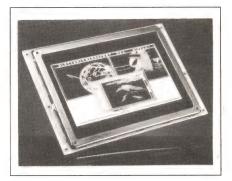
Matrix Corp, 1203 New Hope Rd, Raleigh, NC 27610. Phone (919) 833-2000. FAX 919-833-2550.

Circle No. 359

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- EL display operates with CGA and EGA controllers

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CIRCLE NO. 111

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- Provides performance analysis and real-time test coverage

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available for a variety of target machines, including the 8051, DS5000, 68000, and 68HC11 families, as well as Z80, 64180/Z180, and 8085 processors. SourceGate, \$3000; performance-analysis card, \$2495.

Huntsville Microsystems Inc, Box 12415, Huntsville, AL 35802. Phone (205) 881-6005. FAX 205-882-6701. Circle No. 361

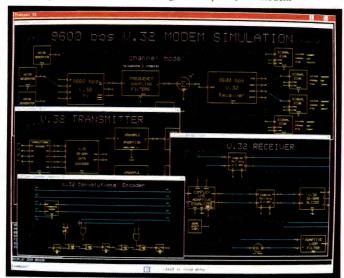
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- Requires no extra hardware
 The VM/386 MultiUser Starter's

The VM/386 MultiUser Starter software package lets you attach two serial text-based terminals to the built-in COM ports of an 80386based PC to obtain a 3-user system

that is completely compatible with PC-DOS. All three users get their own copies of DOS, Autoexec, and Config files and may use terminateand-stay resident programs. Each user can also use Alt-Ctrl-Del to reboot without affecting any other user. The package comes with a PC terminal-emulation program that lets you attach an IBM PC or compatible, instead of a terminal, to the host. If you need to accommodate more than three users, you can upgrade to VM/386 MultiUser, which allows you to attach as many as 32 text-based or graphics terminals, or PCs. For the Starter package, you'll only need to install additional serial ports in the host if both COM ports are already in use for serial devices. For the Multiuser package, you'll need to install boards that will

Block Diagram Editor windows showing hierarchy of V32bis modem



NOW SAVE HUNDREDS OF HOURS IN DSP AND COMMUNICATIONS DESIGN TIME.

provide the appropriate number of serial ports. VM/386 MultiUser Starter, \$395; VM/386 MultiUser, \$895.

IGC, 4800 Great America Pkwy, Santa Clara, CA 95054. Phone (408) 986-8373. FAX 408-986-1431.

Circle No. 362

Windows LAN Print Manager

- Lets you choose local or shared printer
- Summarizes availability and status for each network printer
 Windows Print, Manager lets, w.

Windows Print Manager lets you access and directly control all network printing resources within any Windows application program. You can select either a locally attached printer or any of the shared printers on the LAN; the Print Manager issues all the commands needed to direct output to the selected net-



work printer and can send these across network servers and widearea networks. You name printers descriptively (for example, Multibin Laser Printer in Accounting), and then you can sort the list of printers by name, printer type, or location. A queue manager lets you view the status of your jobs in the print queue; depending on your LAN privileges, you can add, modify, delete, or hold any of your print jobs while other Windows applications continue to run. A notifying feature automatically informs you when one

of your jobs has been printed. You can get context-sensitive on-line help for any Print Manager function, and you can customize the messages. \$695 for a 100-user, single file-server license.

Automated Design Systems Inc, 375 Northridge Rd, Suite 270, Atlanta, GA 30350. Phone (404) 394-2552. Circle No. 363

High-Speed Data-Acquisition Software

- Lets you plot waveforms during streaming
- Continuously stores data to disk with no gaps

Snap-Stream software can store millions of data points to disk in one continuous stream, and it eliminates the gaps that normally occur when acquiring large amounts of data at high speeds because of the 32,000-point DMA-transfer limita-

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Because the Signal Processing Work-System™ automatically converts designs into error-free simulation code, you spend your time designing systems, not debugging programs.

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SPW is the only complete, graphical software for all phases of DSP and communications product design, simulation and implementation. And now with its

of more than 200 function blocks, SPW's range of design capabilities is broader than ever.
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tion of IBM PC/XT and PC/AT computers. On a 386-based computer with a 25-MHz clock, transfer rates can be as high as 88 kHz to a hard disk, 200 kHz to a RAM disk, or 71 kHz to either medium if you want simultaneous plotting. The quantity of data is limited only by the capacity of the storage medium in use. During acquisition you can acquire as many as 80 waveforms and display as many as 32 of these on the screen; at any time you can switch to a new display page (of which there are five) to show a different set of waveforms. The package employs autosensing to predict the system's probable throughput limit, and pretesting of the streaming parameters to avert overrun and loss of data. The built-in disk optimizer arranges the files on disk so that new data will use contiguous sectors. You'll need the vendor's SnapShot Storage Scope software

to run Snap-Stream. Snap-Stream, \$495; Snap-Stream with SnapShot, \$890.

HEM Data Corp, 17336 12 Mile Rd, Southfield, MI 48076. Phone (313) 559-5607. FAX 313-559-8008.

Circle No. 364

A Spice For All Seasons

- Runs on all Macintosh computers
- Needs only 1M byte of RAM
 Compatible with Berkeley Spice
 2G.6, the IsSpice 1.5 enhanced
 simulator runs on any Macintosh
 computer that has as little as 1M
 byte of RAM. The Professional version requires a math coprocessor
 and simulates approximately 1000
 components or nodes/M byte of
 RAM; a version that does not require a math coprocessor has a fixed
 memory limit and can simulate 150
 to 200 nodes. Both versions require

system version 6.03 or greater and Multifinder 6.03, or Multifinder 6.1 alone. You can abort a simulation at any time and save all the analysis data generated up to the time of cancellation. The program accepts input from any popular schematiccapture package, as well as ASCII netlist entry, and provides the following types of analysis: DC, transfer function, sensitivity and curve families, AC, noise and distortion, and transient (including nonlinear time-domain solution with FFT). The package comes with a number of device models and a comprehensive Spice reference manual. Professional version, \$210; noncoprocessor version, \$95.

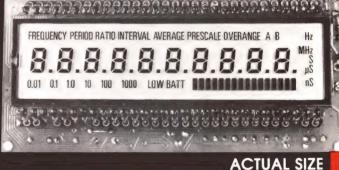
Intusoft, Box 6607, San Pedro, CA 90734. Phone (213) 833-0710.

Circle No. 365

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626	6 D/A	16	Servos, Robotics	



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119 Russell Street, Suite #6 Littleton, MA 01460

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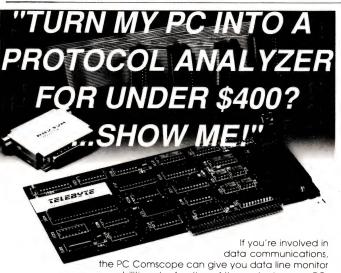
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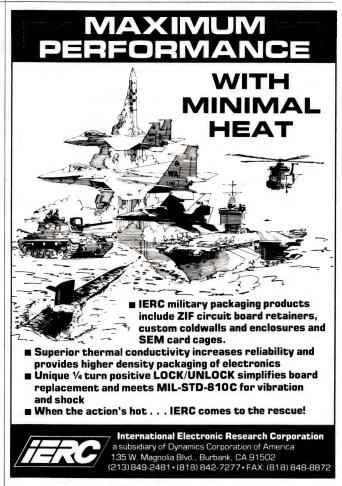


capabilities at a fraction of the cost using your PC. Making use of pull down menu's and built-in help screens provides true operator simplicity. The combination of these features and price make this an extraordinary buy. You can view the bidirectional data and control signals of any RS-232 link. The PC Comscope capabilities include: ASYNC; SYNC; HDLC; TIME STAMPING; SOPHISTICATED TRAPPING; STORE DATA ON DISK; ASCII; EBCDIC; IPARS.... Telebyte does it again!

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CIRCLE NO. 116



CIRCLE NO. 117

NEW PRODUCTS

INTEGRATED CIRCUITS

Dual 14-Bit S/D Converter

- Comes in a small 28-pin double DIP
- Velocity output eliminates tachometer

Packaged in a small, hermetic 28pin double DIP, the SDC-14600 hybrid IC contains two 14-bit S/D (synchro to digital) converters. A velocity output eliminates the need for a tachometer and provides a ground-referenced 4V signal with an accuracy of 4 minutes and a linearity of 1%. Available input options include an 11.8V resolver, an 11.8 or 90V synchro resolver, or a



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2V direct resolver. The input frequency range is 360 Hz to 5 kHz, and the closed-loop bandwidth is 100 Hz. The digital outputs of the SDC-14600 are buffered with a 3-state transparent latch, which allows the transfer of data without disturbing the converter's tracking of input signals. The SDC0-14600 is available in commercial and military temperature ranges. From \$565 (1 to 9). Delivery, 30 to 60 days ARO.

ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716. Phone (516) 567-5600. FAX-516-567-7358. Circle No. 378

Telephone Chip

- Controls all keypad operations
- Includes three 24-bit memories
 The MTC-2094 is a telephone control chip, which the company calls a BORIS (bit flag oriented reduced instruction set) controller. Using the single chip, you can control all keypad operations and produce either dial tones or pulse signals. Incorporated are three 24-bit memories that you can manipulate for automatic use and last-number redialing. Ceramic 28-pin DIP version, \$4.25; plastic leaded chip carrier version, \$4 (1000). Available in the second quarter of 1990.

Mietec, Zone d'activities de Courtaboeuf, 6 avenue de Norvege, 91953 Les Ulis, France. Phone 1 69 074054. FAX 1 69 076664.

Circle No. 379

Text continued on pg 202

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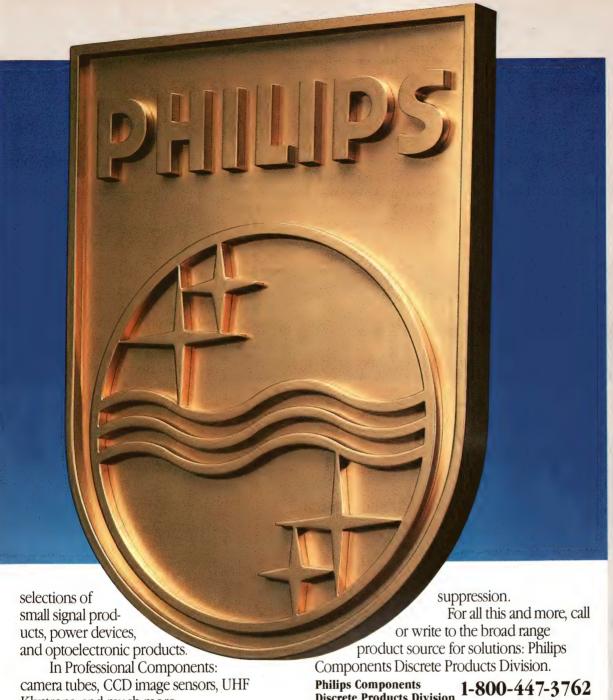
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- Available in TO-257 packages

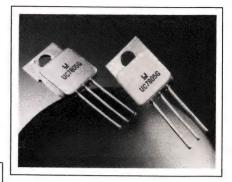
The UC78XXX and UC79XXX series of 3-terminal voltage regulators come in hermetic, metal TO-257 packages suitable for military applications. Compared with standard TO-3 metal packages, the TO-257

MiniModule/SSP.

offers lighter weight, a lower profile, and smaller size. The nonisolated, fixed-voltage UC78XXG and UC79XXG series are positive and negative regulators rated at 1.0A. Available in 5, 12 and 15V versions, these regulators have an output tolerance of +4%. The UC78XXAG and UC79XXAG have +1% toler-

MiniModule/Modem:

MiniModule/LCD; Controller for 640 X 200



ance. The series of isolated-tab versions are designated 78XXIG and 79XXIG (4%) or 78XXIAG and 79XXIAG (1%). Other regulators in the family include adjustable types such as the UC117G and UC150G (positive) and UC137G (negative). Fixed-voltage types, from \$16.74; adjustable types, from \$22.15 (1000).

Unitrode Integrated Circuits Corp, 7 Continental Blvd, Merrimack, NH 03054. Phone (603) 424-2410. Circle No. 380

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Mobile-Radio Audio Chip

- Controlled by a μP
- Comprehensive filter selections The FX506 combines the essential circuits for audio processing in a mobile radio. You control the various elements with a 47-bit data word entered serially from a host μP. The FX506's input multiplexer feeds signals to an input amplifier having a gain of 15 dB, adjustable in 1-dB steps. Next, the signal passes through a compression circuit to speech-band filters preset to 300 Hz and 3 kHz. Finally, the signal goes to a fine gain-adjust amplifier with 0.25-dB increments. For further processing you can select pre- and de-emphasis filtering centered around 1 kHz with a 20-dB/ decade roll-off. You can also switch in a separate deviation limiter (2.55) to 3 kHz) to satisfy differing channel-spacing requirements. An output multiplexer feeds your VCO reference and VCO drive channel, which includes a programmable 48dB attenuator. For noise-squelch

control you have a separate path, sourced either from the input signal or the received signal-strength indicator in the radio. Your control program can turn off unneeded functions to save power. Offered in either a DIP, surface-mount, or chip-carrier package. £6.85 (1000).

Consumer Microcircuits Ltd, 1 Wheaton Rd, Whitham, CM8 3TD, UK. Phone (376) 513833. FAX 376-518247. Circle No. 381

Current-Conveyor IC

- Wide bandwidth
- Low distortion

Designed for use in professional audio applications, the PA6330 and PA630A each contain an accurate (0.5%) current conveyor, a current mirror, and two unity-gain buffer amplifiers. The current-conveyor section has a bandwidth of 18 MHz and distortion of only 0.02%. The bandwidth of the buffer amplifiers is 50 MHz. The PA630A has two additional pins, which you can use to interface with two external JFETs for enhanced performance. In addition to their use as gain blocks and inverters, you can use the PA630/630A to implement a virtual-ground input without the global negative feedback required by most other circuits such as op amps. PA630 in 16-pin DIP, \$8.42; PA630A in 18-pin DIP, \$8.89 (100).

Phototronics, Box 977, Manotick, Ontario, Canada K0A 2N0. Phone (613) 692-2247. FAX 613-692-2605. **Circle No. 382**

Intelligent Power Drivers

- For automotive applications
- 5-pin TO-220-FM package

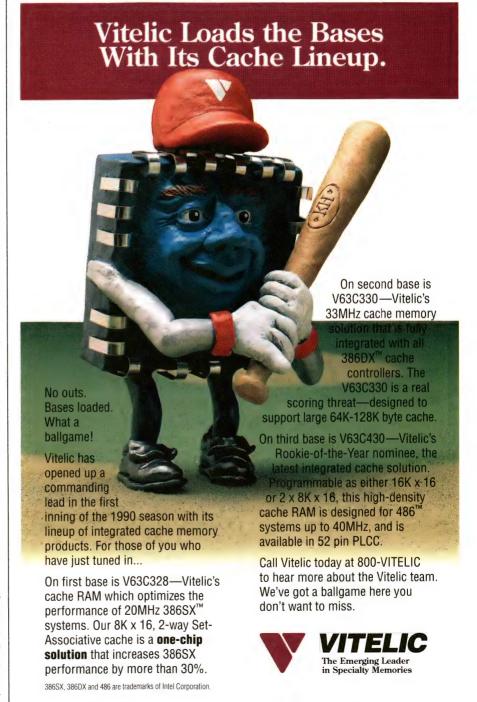
Combining digital logic and power transistors on a single chip, the HA13702A lamp driver and HA13703A solenoid driver reduce the number of components needed in automotive electronic systems. The devices are also useful in motor-control and power-supply appli-

cations. Both devices can withstand a 60V load dump and feature protection against voltage, current, and temperature overloads. The normal operating voltage range is 7 to 25V, and output current capability is 4A. A TTL-compatible output allows communication of system status and diagnostic messages.

Available in 5-lead TO-220-FM packages, the devices operate from -40 to $+125^{\circ}$ C. HA13702A, \$3.25; HA13703A, \$3.50 (1000).

Hitachi America Ltd, Semiconductor & IC Div, 2000 Sierra Point Pkwy, Brisbane, CA 94005. Phone (415) 589-8300. FAX 415-583-4207.

Circle No. 383



Circle 14 for literature

Circle 15 for sales contact

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High-Voltage DC/DC Converters

- Have a 10V dc standard input
- Feature short-circuit protection

D Series high-voltage dc/dc converters have a standard input of 10V dc, but units are available that will accommodate inputs of 5 to 28V dc. Standard output capabilities range from 100V at 250 µA to 1200V at 100 µA. A regulated output option is available for units with outputs of 500V or less. The modules feature RFI filtering/shielding and come with short-circuit protection as a standard feature. MTBF measures in excess of 100,000 hours. From \$52.25.

EMCO High Voltage Co, 11126 Ridge Rd, Sutter Creek, CA 95685. Phone (209) 223-3626. FAX 209-223-2779. Circle No. 366

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WITH NO EXTERNAL PARTS

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MTTF

New



2-Wire Current **Transmitter**

- Supports 2- or 3-wire platinum RTDs
- Features RFI/EMI shielding Fully isolated at 600V ac or dc, the IXMIT-RTD 2-wire transmitter operates at 4 to 20 or 10 to 50 mA and supports 2- to 3- wire, 100Ω platinum RTDs (resistance temperature detectors). Operating from any 12

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Acculex, 440 Myles Standish Blvd, Taunton, MA 02780. Phone (508) 880-3660, TLX 503989,

Circle No. 367

Miniature Inductors

+85°C, and Q values range to 50. Delivery,

Jefryn Blvd E, Deer Park, NY 11729. Phone (516) 586-5566. FAX 516-586-5562. Circle No. 368

• Compatible with

automatic-insertion equipment • Have Qs of 50

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Renco Electronics Inc, 60

The lowest noise general-purpose DC/DC Converter on the market, the PWR1546A offers a maximum noise of just 1.0mV p-p

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CIRCLE NO. 124

1W DC/DC Converters

- Available in SIP and DIP housings
- Have an 80% efficiency NME Series 1W dc/dc converters feature a 20W/in.3 power density.

They provide isolated outputs of 5,

EDN March 1, 1990

12, and 15V from inputs of 5 and 12V. Units come in SIP as well as industry-standard 8-pin DIP housings. The converters operate over a -25 to +70°C range and have an efficiency of 80%. Input-to-output isolation measures 500V dc. \$19.50.

International Power Sources Inc. 200 Butterfield Dr. Ashland. MA 01721. Phone (508) 881-7434. FAX 508-879-8669.

Circle No. 369

PNP Audio Transistors

- Have a 190-MHz bandwidth
- Include internal-protection diodes

SSM-2220 dual matched pnp transistors have an input-voltage-noise rating of $0.7 \text{ nV}/\sqrt{\text{Hz}}$ over a bandwidth of 20 Hz to 20 kHz. The units have a 190-MHz bandwidth and a maximum offset of 200 µV. Current-gain matching of 0.5% helps reduce high-order amplifier harmonicdistortion figures. The package includes protection diodes across the base-emitter junction to clamp any reverse breakdown potentials. The bulk resistance measures 0.3Ω typ to ensure accurate logarithmic conformance. Housed in an 8-pin epoxy DIP, the transistors operate over a -40 to +85°C range. \$1.95 (100).

Precision Monolithics Inc. Box 58020, Santa Clara, CA 95052. Phone (408) 727-9222. FAX 408-727-1550. Circle No. 370

Lightning Protector

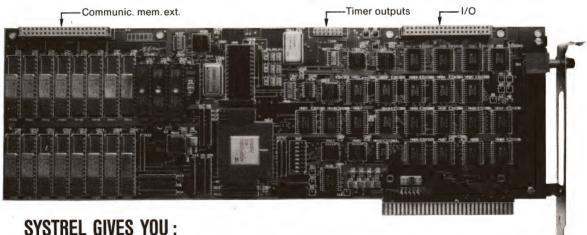
- Works with any RS-232C interface
- Handles both synchronous and asynchronous applications

Accommodating either synchronous or asynchronous applications, the model 341 lightning protector pro-

vides 3-stage protection for 11 signal lines of any RS-232C interface. The three stages include highpower gas tubes and two stages of avalanche diodes. The tubes are inductively isolated from the diodes. which are resistively isolated from each other. The units limit the effects of any lightning strike to less than the ± 25 V limit of the RS-232C specification, and the reaction time is <1 nsec. Each interface port includes both female and male connectors. These built-in gender changers also provide users with a monitor port. Dual earth-ground connection studs help provide a low-inductance path for the lightning surge. \$198.

Telebyte Technology Inc, 270 E Pulaski Rd, Greenlawn, NY 11740. Phone (516) 423-3232. FAX 516-Circle No. 371 385-8184.

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CIRCLE NO. 126 205 EDN March 1, 1990

LITERATURE

Connectors categorized

The company's 1990 Connector Source Book features a wide selection of connectors, including D subminiature, zero-insertion force, edgecard, rack and panel, automotive, fiber optic, microminiature, MIL-SPEC, RF, and coaxial. The book also contains a complete list of company locations throughout North America.

ITT Cannon, 1851 Deere Ave, Santa Ana, CA 92705.

Circle No. 372



Booklet highlights motion-control systems

The manufacturer's 8-pg brochure surveys its brushless motion-control systems. The publication explains that a special function of the MCS-S Series is the ability to provide electronic line shafting for as many as 32 servomotors.

Ormec, 19 Linden Park, Rochester, NY 14625. Circle No. 373

Connecting sensors to analog input boards

The vendor's 12-pg guide, Interfacing Sensors to Analog Input Boards, helps you connect a variety of sensors to general-purpose analog input boards. The listing of boards includes DAD-48, AD1260, and AD816, but the examples given are also applicable to analog boards from other vendors. The types of sensors included in the publication consist of unpowered, self-powered, and externally powered 4- to 20-mA transmitters, strain gauges, and resistive bridges; resistance-temperature detectors; solid-state temperature sensors; thermocouples; and current transformers.

Computer Dynamics Sales, 107 S Main St, Greer, SC 29650.

Circle No. 374

Handbook on fiber-optic sensors

According to the ISA (Instrument Society of America), its reference handbook, Fiber Optic Sensors— Fundamentals and Applications, combines scientific method with engineering-design good proaches to solve practical instrumentation problems. **Subjects** from Snell's range law and Maxwell's equations to Mach-Zehnder interferometry and laser Doppler interferometry. The publication discusses single- and multimode fibers, the sensitivity and dynamic response of fiber-optic sensors, expected performance, limitations, and noise problems. The volume also discusses the advantages and disadvantages of many sensor configurations. For ISA members, \$36; for nonmembers, \$44.95.

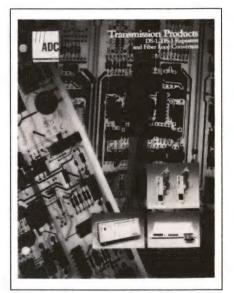
Instrument Society of America, Box 12277, Research Triangle Park, NC 27709. Circle No. 375

Article covers fluoropolymer coatings

The technical article, Thick and Thin Film Fluoropolymer Functional Coatings, presents an overview of the most commonly used fluoropolymer coatings. The document discusses six major fluororpolymer coating materials, giving the advantages and disadvantages of each. The publication describes basic properties of each fluoropolymer, including temperature parameters, abrasion resistance, corrosion resistance, tensile strength, and creep resistance. Further, the article posits typical applications. A problem-solving section deals with abrasion and corrosion resistance, friction, and mold release.

The ISPA Co, 2915 Wilmarco Ave, Baltimore, MD 21223.

Circle No. 376



Listing of transmissions

The vendor's 4-color Transmission Catalog features a wide range of specialty transmission products for maintenance and transport, such as DS0-1 and DS-3 repeaters, and the fiber-loop converter. Schematics indicate where transmission products fit in a telecommunications network. The book also provides extensive product and application information, as well as technical specifications.

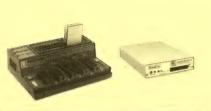
ADC Telecommunications, 4900 W 78th St, Minneapolis, MN 55435.

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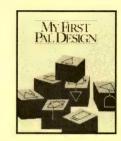
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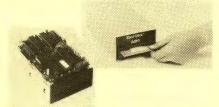
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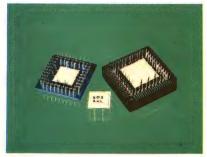
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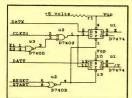


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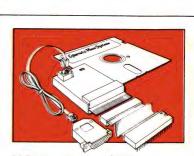
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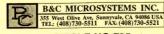
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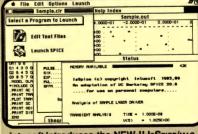
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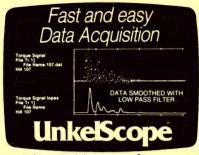


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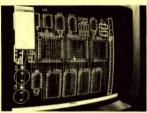
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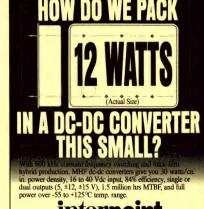
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CAREER OPPORTUNITIES

EDN Magazine Edition News Edition

1990 Recruitment Editorial Calendar

Issue	Issue Date	Ad Deadline	Editorial Emphasis
Magazine Edition	Mar. 29	Mar. 8	Software Special Issue—Interface ICs, Software/Programming/Microprocessors/ASICs, April Fools Section, Special Design Project #2
News Edition	Apr. 5	Mar. 16	IC/Logic ICs, Distribution, Special Supplement: Distribution
Magazine Edition	Apr. 12	Mar. 22	Communications Special Issue—Communication ICs, Communication Systems, Microprocessors, Special Design Project #3
News Edition	Apr. 19	Mar. 30	ICs/Graphics Controllers/Microprocessors, Industrial Automation, Regional Profile: So. California
Magazine Edition	Apr. 26	Apr. 5	Computer Boards/Microprocessors, Power Sources, Sensors/Transducers, Special Design Project #4, Electro Show Issue
News Edition	May 3	Apr. 12	CAE/Board Layout, Education, Special Supplement: ASICs, Electro Show Issue
Magazine Edition	May 10	Apr. 19	Analogy Technology Special Issue—Analog ICs, Analog Instruments, Digital ICs/ Microprocessors/ASICs, Special Design Project #5
News Edition	May 17	Apr. 27	ICs/Memory ICs, Test & Measurement, Regional Profile: Massachusetts & New Hampshire
Magazine Edition	May 24	May 3	Microprocessors, Computers & Peripherals, Semicustom ICs/ASICs, Components, Sensors & Transducers
Magazine Edition	June 7	May 17	Software, Design Tools, Microprocessor I/O Chips, μP Support Chip Directory
News Edition	June 14	May 24	Peripherals/Input Devices, Software, Special Supplement: EDA
Magazine Edition	June 21	May 31	Computer-Aided Engineering, Computers & Peripherals, Power Semiconductors, Semicustom ICs/ASICs
News Edition	June 28	June 8	ICs/RISC/Microprocessors, Image Processing, Regional Profile: Oregon & Washington
Magazine Edition	July 5	June 14	Product Showcase—Volume I: Hardware & Interconnect, Power Sources, ICs & Semiconductors, Software
News Edition	July 12	June 21	Analog/Communication ICs, ASICs, Special Supplement: Automotive Electronics, Regional Profile: Washington, D.C.
Magazine Edition	July 19	June 28	Product Showcase—Volume II: CAE/ASICs, Computers & Peripherals, Components, Test & Measurement
Magazine Edition	Aug. 2	July 12	Digital ICs/Microprocessors, Computer-Aided Engineering, Computers & Peripherals, Test & Measurement, Technical Article Database
News Edition	Aug. 9	July 20	CAE/Software, Aerospace, Special Supplement: Defense
Magazine Edition	Aug. 20	July 30	Military Special Issue, Vision/Image Systems, ICs & Semiconductors, Memory Technology, Software
News Edition	Aug. 23	Aug. 3	Electromechanical, Opportunities in Non-EOEM, Regional Profile: New Mexico, Arizona
Magazine Edition	Sept. 3	Aug. 13	ASICs Special Issue—Semicustom ICs, Computer-Aided Engineering, Digital Components, ICs & Semiconductors
News Edition	Sept. 6	Aug. 17	CAE/Software, CASE/CAE, Special Supplement» DSP
Magazine Edition	Sept. 17	Aug. 27	System Software, Computer-Aided Engineering, Analog ICs, Digital ICs
News Edition	Sept. 20	Aug. 30	ICs/Non-volatile Memory, Fiber-Optics, Regional Profile: Georgia, N. Carolina & Alabama

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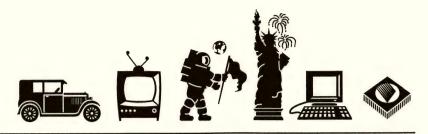
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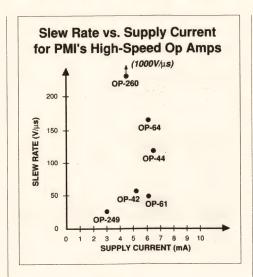
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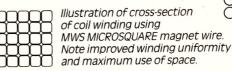
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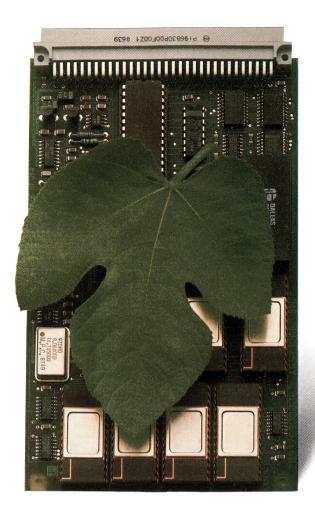




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